NADC-80014-60

LEVEL

270 VDC VARIABLE SPEED GENERATOR AND CONTROL UNIT, AIRCRAFT ELECTRIC POWER SYSTEM

AiResearch Manufacturing Company of California
A Division of The Garrett Corporation
2525 West 190th Street
Torrance, California 90509

1 May 1980

TECHNICAL REPORT NADC-80014-60
Final Report

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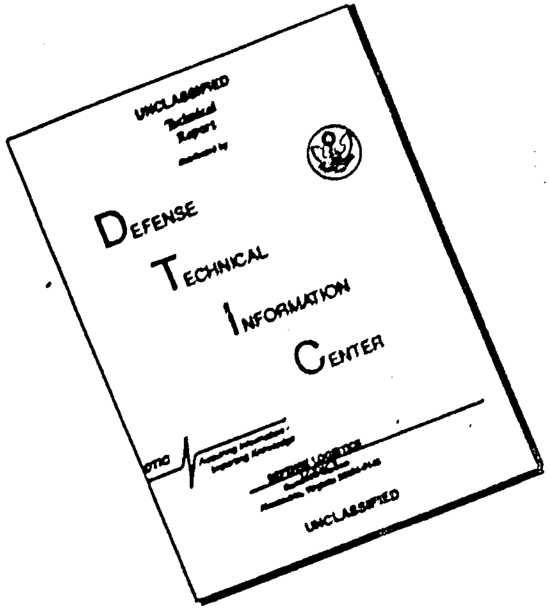

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The program objective was to develop a 270 vdc, 45 kw generator-controller system for a 9,000 to 18,000 rpm speed range, and to establish a data base sufficient to prove the feasibility of a 270 vdc electrical system as the primary aircraft electrical power. The 270 vdc system developed by AiResearch consists of a permanent-magnet generator with an internal cooling and lubricating

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system, a phase delay controlled thyristor rectifier, and a microprocessor-monitored protection unit. Functional requirements of the detail specification, including ripple and transient voltages, were successfully met. The feasibility and the advantages of the permanent-magnet generator/phase-delay rectifier-regulated system were demonstrated.

NADC-80014-60

AIRESEARCH MANUFACTURING COMPANY
OF CALIFORNIA

270 VDC VARIABLE SPEED
GENERATOR AND CONTROL UNIT,
AIRCRAFT ELECTRIC POWER SYSTEM

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PREFACE

The AiResearch Manufacturing Company, a Division of The Garrett Corporation, submits this final report to the Naval Air Development Center, Warminster, PA 18974, to fulfill the requirements of Contract N62269-76-C-0223, item 0002. This document describes the technical progress during the program resulting in the shipment of one 270 VDC, 45 KW Generator-Control Unit System. AiResearch appreciates the technical guidance and encouragement received from Mr. Howard Ireland and Mr. Joseph Segrest of NADC.

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ABBREVIATIONS AND SYMBOLS

ANSYS	Analysis system
CMOS	Complementary metal oxide semiconductor
CS	Current sensor
CT	Current transformer
EMI	Electromagnetic interference
EPROM	Erasable programmable read-only memory
T_{tu}	Ultimate strength
T_{ty}	Yield strength
GCU	Generator control unit
GLC	Generator line contactor
HIP	Hot isostatic pressure
I/O	Input/output
IPT	Interphase transformer
Ksi	Kilopounds per square inch
L-C	Inductive-capacitive
L-L	Line-to-line
L-N	Line-to-neutral
MS	Margin of safety
PC	Printed circuit
PDR	Phase-delayed rectifier
PU	Per unit
RAM	Random-access memory
SCR	Silicon-controlled rectrifier
TTL	Transistor transistor logic
σ_{all}	Allowable stress
σ_{app}	Applied stress

SECTION 1

SUMMARY

PURPOSE AND GOALS

The purpose of this program was to develop a variable speed generator-controller system for 270 vdc primary aircraft power applications. The goals were to prove the feasibility and the advantages of a permanent-magnet generator working with a phase-controlled thyristor rectifier and microprocessor control unit, and to establish a data base sufficient to carry the 270 vdc program into the next phase of system distribution and interface tests.

PROGRAM ACCOMPLISHMENTS

A system was designed, components and subsystems were developed and tested, hardware was fabricated, and system tests were conducted and completed on one generator and one generator-control unit before shipment. Figures 1-1, 1-2 and 1-3 show the system components as shipped after final testing. Figure 1-2 also shows the interconnecting cable assemblies and the test panel necessary for system troubleshooting, checkout, and operation.

PROGRAM HIGHLIGHTS

Program highlights included the following:

ROTATING MACHINE

- Successful design and manufacture of the highly sophisticated main housing, the manifold castings, and the hot isostatic pressure-bonded rotor assembly
- Successful design and test of the cooling system pitot pump
- Demonstration of the ability to regulate output voltage to 270 vdc under all load and speed combinations, and to limit ripple and transient voltages to specification values

POWER ELECTRONICS

- Successful design and fabrication of a high-temperature high-frequency phase delay rectifier using standard available technology and sophisticated application engineering.
- Development of a special package thyristor for oil cooling

GENERATOR CONTROL UNIT

- Designed and demonstrated the feasibility of controlling (2) phase-delayed rectifiers summed through an interphase transformer

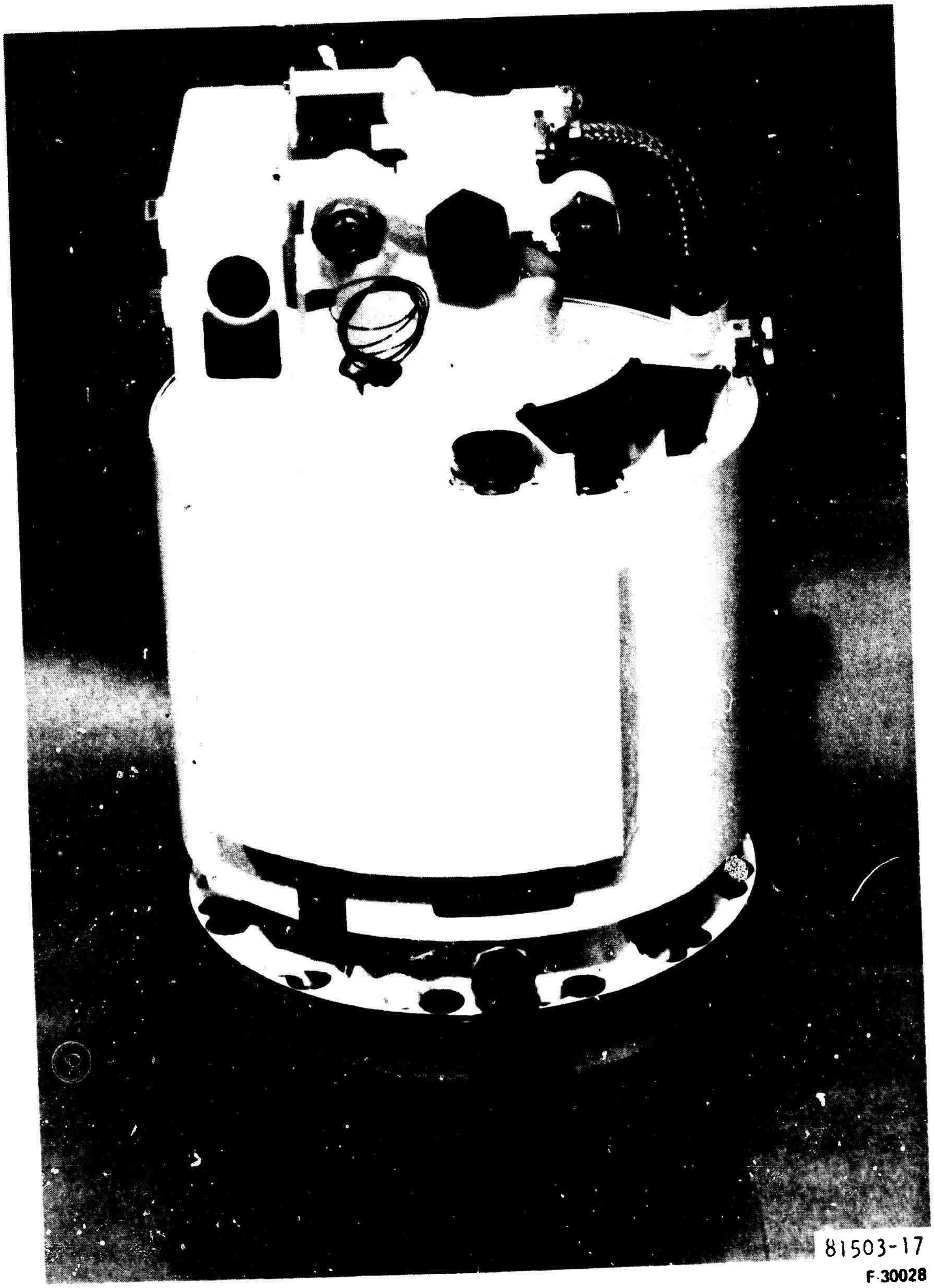

Figure 1-1. 270 VDC Permanent Magnet Generator

- Designed control circuitry to control the phase-delayed rectifiers at high frequency and keep output ripple within specified requirements.

- Designed a microprocessor-based fault detection system, capable of starting and shutting down the generator and associated generator line contactors, based on the distribution system health.

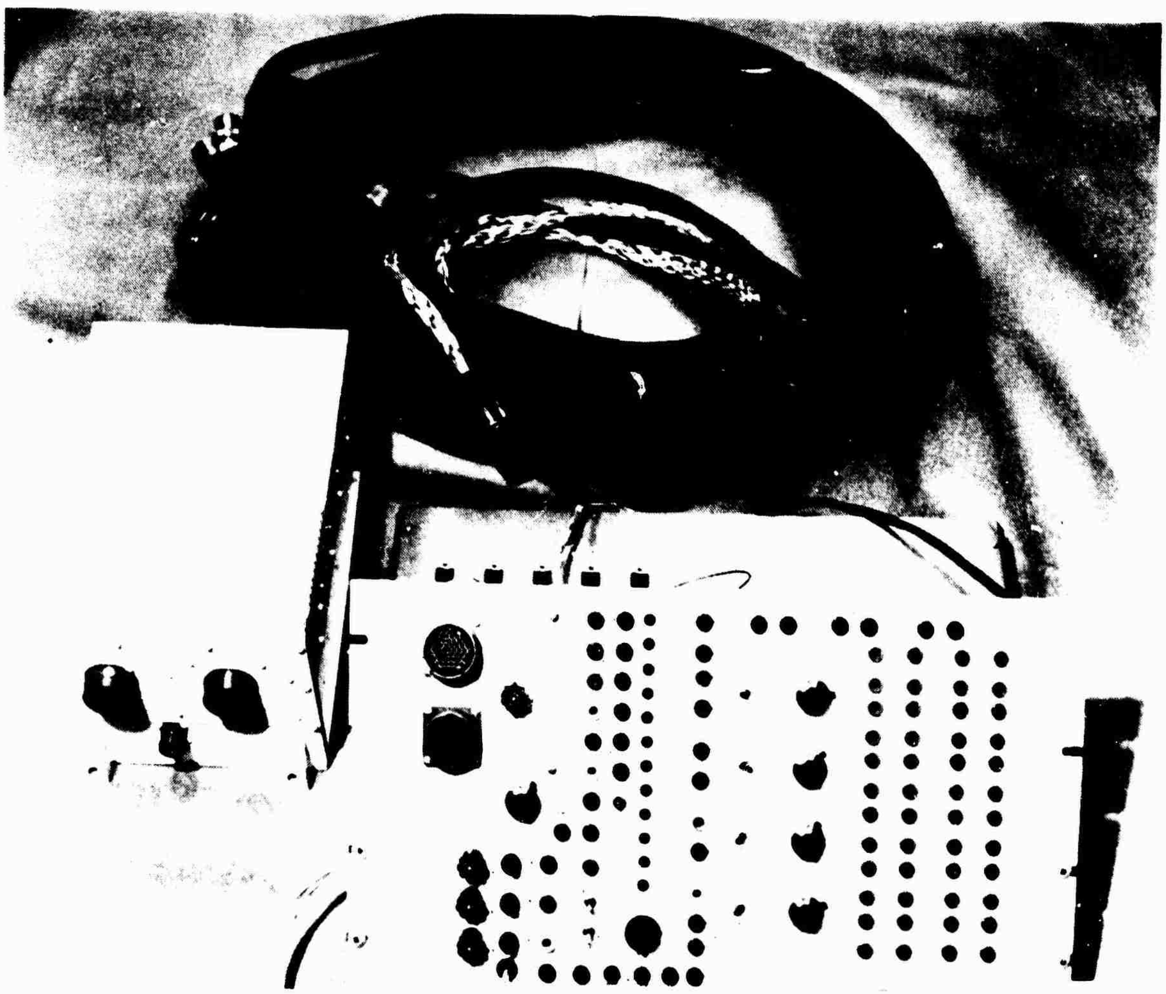

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Figure 1-2. Generator Control Unit With Connecting Cables and Test Panel

WORK ACCOMPLISHED

Table 1 provides a brief summary of all work done on the program and makes reference to the section of the report wherein the subject is discussed in detail.

SYSTEM LIMITATIONS

In order to circumvent possible problem areas that were not directly associated with the demonstration of the feasibility of the 270 vdc generating system, several design parameters such as overspeed, short-circuit protection, 150-percent load switching, high-temperature coolant inlet and ambient, were not tested at full stress level. A detailed discussion of the test conditions is presented in Section 5, Performance Verification.

TECHNOLOGY DEVELOPED

The feasibility of an electronically controlled high-speed permanent-magnet generator for the 270 vdc primary aircraft electrical system has been firmly established. There should be no fundamental problems in adapting this technology to further systems development.

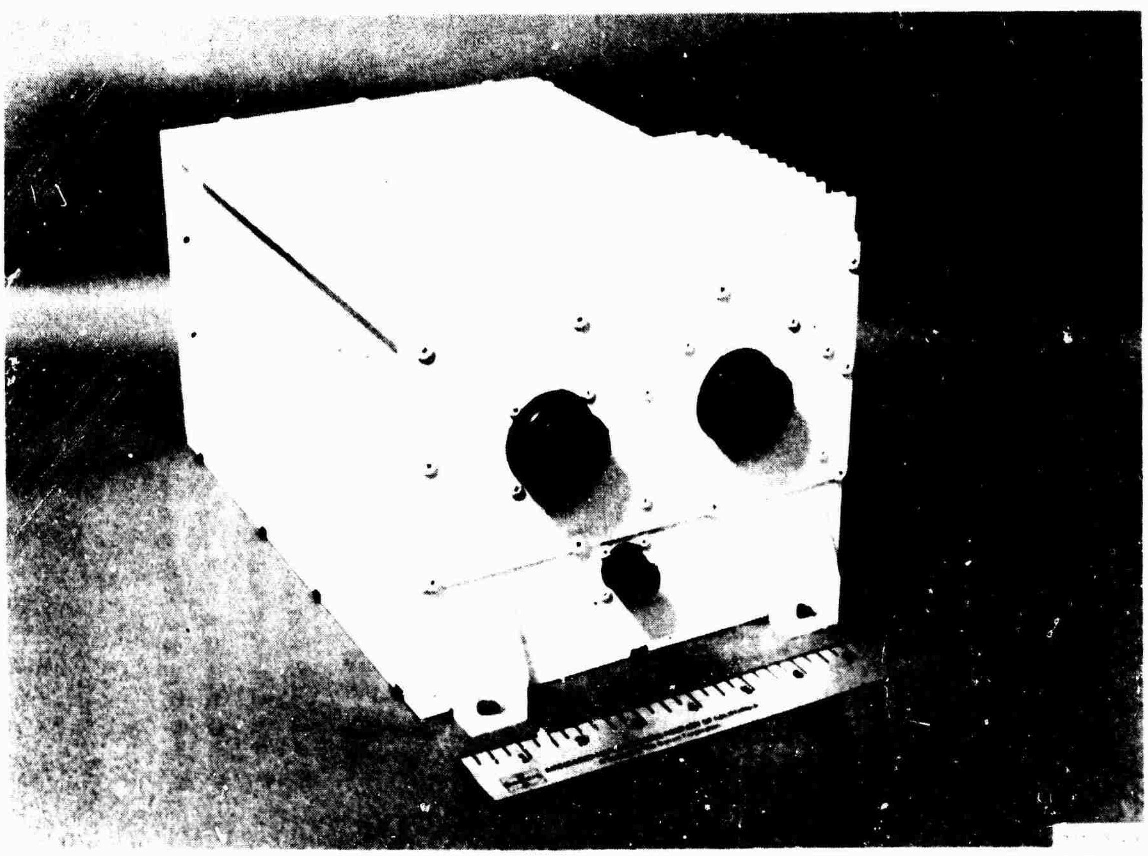

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Figure 1-3. Generator Control Unit

TABLE 1-1 WORK ACCOMPLISHED

Tasks and Subtasks	Page(s) Discussed
ROTATING MACHINE	
Analytical Evaluation	
• Electromagnetic design of rotating machine, using computer model optimization program	4-76 to 4-85
Stress Analysis	4-1 to 4-5
• Rotating assembly--fabrication and dynamic considerations	5-1 to 5-4
• Structural integrity of static members	4-1 to 4-3
Thermal Analysis	
• Rotating machine	4-6 to 4-12
• Power electronics	4-8, 4-13
• Generator	4-6, 4-7
• Generator control unit (GCU)	4-19 to 4-28
• Cooling loop pressure drops, flow requirements	4-8
• Pitot Pump design	4-79, 4-85 to 4-87
• Coolant optimization	2-2, 4-8
System Layout	
• Assembly drawing	3-4 to 3-7
• Outline drawing	3-8, 3-9
• Interconnecting electrical diagram	3-2
• Detail drawings	3-11, 5-7 to 5-9, 5-23, 5-25

TABLE 1-1 (Continued)

Tasks and Subtasks	Page(s) Discussed
Hardware and Fabrication	
Airborne Equipment	2-1, 2-2
• Two rotating machines, one extra stator stack	
• Six extra magnets	
• Two extra bore seals	
• Four extra main housing castings	
• Four extra manifold castings	
• Six extra thyristor assemblies	
• Six extra bearings	
• Generator fabrication and assembly tooling	
• Two generator control units	
Test Equipment	A-1
• 270 vdc load bank	A-1
• Generator adapters and mounting plates	A-1
• Generator control unit test panel	A-1 to A-6
• Hydraulic servicing and heat exchanger system	A-6 to A-9
Performance Verification	
Component and Subsystem Tests	
• Pitot pump development tests	5-22, 5-23, 5-24
• Component pressure drop and flow tests	5-5, 5-10, 5-11
• Rotor assembly overspeed tests	5-1, 5-3, 5-4
• Generator mechanical integrity tests	5-1, 5-21
• Electrical performance tests	5-12 to 5-40

TABLE 1-1 (Continued)

Tasks and Subtasks	Page(s) Discussed
System Testing	
• Generator-GCU interface development	5-22
• Load regulation	5-34, 5-35
• Ripple voltage	5-36, 5-37, 5-38
• Switching transients	5-39, 5-40
• Efficiency	5-36, 5-37, 5-38
POWER ELECTRONICS	
Analytical Evaluation	
• Alternator power circuit design, using computer model	4-8, 4-76
• Power electronics component design also optimized by computer model	4-14
Stress Analysis	
• Stress levels for voltage, current, shock, vibration and temperature shock determined and specified for power circuit components	4-2, 4-3, 5-12
Thermal Analysis	
• Best cooling method for each power circuit component determined by thermal analysis	4-10, 4-14, 4-15
Power Circuit	
• Hardware configuration	4-15 thru 4-18
• Schematic diagrams	3-20, 3-21
• Wiring diagrams	4-13

TABLE 1-1 (Continued)

Tasks and Subtasks	Page(s) Discussed
Power Circuit Hardware	
• 36 Thyristors (546306)	4-14 thru 4-19
• 3 Capacitors (546309)	
• 3 Inductors (546310)	
• 36 Transformers (546311)	
• 3 Transformers (2047031)	
• 3 PC Boards (546315-1)	
GENERATOR CONTROL UNIT	
Analytical Evaluation	4-19 thru 4-76
• Analytical evaluation of control concepts using analog computer simulation of SCR bridge and load impedances	
• Evaulation of packaging methods, trading thermal, vibration, and EMI requirements	
• Evaluation of 270V instrumentation power supply requirements fed from the generator auxiliary winding	
• Evaluation of the location of circuitry between the generator housing and the GCU chassis	
• Evaluation of possible system configurations which would utilize the 270V generator	
• Flow-charted fault logic requirements and compiled computer programs to implement such logic	
Detailed Circuit Design	4-28 thru 4-78
• Detailed circuit design of all necessary control circuits, power supply, EMI filtering and microprocessor circuitry	
Thermal Analysis	4-19 thru 4-24
• Thermal analysis and trades of various package configurations in order to meet temperature environments	

TABLE 1-1 (Continued)

Tasks and Subtasks	Page(s) Discussed
Packaging	
• Printed circuit board drawings	4-21
• EMI filter drawings	4-27
• Spec control drawings	4-28
• Wire lists	4-29
• Subassembly drawings	4-57
• Final assembly drawings	4-63
• Outline drawings	4-71
• Schematics	4-88
Performance Verification	5-5, 5-6
• Breadboard Development	
• Power supply	
• SCR gate drive circuits	
• Control logic	
• Microprocessor development	
• Microkit development system	
• Software development	
• Packaged GCU development	
• Circuit board development	
• Power supply development	
• Development of unit in electronics lab	
• Software integration using emulator	
• Open-loop tests	

TABLE 1-1 (Continued)

Task and Subtasks	Page(s) Discussed
Performance Verification (Continued)	5-5, 5-6
• System integration	5-22
• Closed-loop tests	
• Microprocessor tests	
Hardware	5-6
Generator control units (2)	1-3, 1-4, 5-29
Microkit	4-44 thru 4-53
• Tape recorders (2)	
• Emulator	
• TV monitor	
• Keyboard	
Test panel	A-1
Cable (system interconnect) (2 sets)	1-3
Current transformers (4)	3-2
Extender PC cards	
PC board test box	
Vendor Liaison	NA
Significant engineering time consumed in liaison with local vendors, where most of the power circuit components were manufactured.	

TABLE 1-1 (Continued)

SECTION 2

SYSTEM SPECIFICATIONS AND DESIGN APPROACH

The initial program requirements were directed toward developing a 270 vdc generating system as a laboratory device capable of demonstrating system feasibility by test cell operation. The basic system goals and the actual program results are given in Table 2-1.

Due to technical problems and funding limitations during the program, changes were made in the secondary requirements--keeping in mind the main program goals. Table 2-2 summarizes the changes which resulted in the final shipped configuration described in detail in the following sections of this report.

TABLE 2-1. PROGRAM GOALS VS RESULTS

Parameter	Specification Goals	Program Results
Rated capacity	45 kw at 9,000-18,000 rpm	45 kw at 9,000-18,000 rpm
Rated voltage	270 vdc	270 vdc
Rated current	166 amps	166 amps
Overspeed for Regulation	19,800 rpm	18,500 rpm
Overspeed for Mechanical Integrity	21,600 rpm	19,000 rpm
Underspeed	7,000 rpm	7,000 rpm
Generator efficiency	85 percent (min)	88.2 percent (min)
System efficiency	80 percent (min)	88.1 percent (min)
Overhung moment	550 lb-in. (max)	TBD
Heat rejection	400 Btu/min. (max)	314 Btu/min
Weight of generator	52 lb (dry)	74.40 lb (dry)
Weight of GCU	5 lb	16.35 lb
Number of systems required	2 systems	One shipped One to be refurbished under separate funding

TABLE 2-2. PROGRAM CHANGES

Parameter	Proposed Configuration	Final Design	Reason for Change
Cooling system	MIL-L-23699	Coolanol 25	Low temperature incompatibility with pump
Lube system	MIL-L-23699, active	MIL-L-23699, wick type reservoir	To separate cooling and lube systems
Quick-disconnect system	Resettable plunger/ integral worm tread	Inertia-disc brake/ screw type	High-speed requirements (eliminated from shipped unit due to test malfunction)
Rotor damper	Copper sleeve	Inconel 718 sleeve	Increased strength and resistance
Auxiliary stator	Ironless axial gap	Iron stator axial gap	Insufficient output with ironless stator
Gate drive assembly	All PDR associated electronics located in generator	Gate drive transformers and diodes only in generator	Insufficient space and cooling
Overspeed	21,600 rpm	19,000 rpm, 5 cycles at 350°F	To reduce program risk
Pressure fill port	MS24476-1 and MS24480-1	Fill cap on top of reservoir	To simplify design
Coolant filter	Located on generator	Located on outside service loop	To simplify service
Seals	Three carbon face seals	One carbon face seal	Changed lube system to reduce losses

SECTION 3

FUNCTIONAL DESCRIPTION

The 270 vdc system developed in this program consists of an integrally cooled permanent-magnet generator/phase-delay rectifier system, controlled and protected by a separate electronic unit, and interconnected as shown in drawing 801577 (Figure 3-1). Key design features and functional aspects of the major subcomponents are described in the following paragraphs.

ROTATING MACHINE

The generator assembly drawing, 518989 (Figure 3-2), shows the salient features of the rotating machine. The outline drawing, 518988, is shown in Figure 3-3. The functional description refers to individual item (find) numbers of the assembly drawing. To clarify the presentation, the rotating machine is described under electromagnetic, mechanical, and thermal design and function headings.

ELECTROMAGNETIC DESIGN AND FUNCTION

Major electromagnetic subcomponents of the generator consist of the main stator assembly (item 7), the rotor assembly (item 8) and the auxiliary stator assembly (item 20).

The main electrical output stator assembly uses a 72-slot, thin silicon steel laminated stack. The laminations are individually insulated and bonded to form the stack assembly. The stator winding consists of two evenly distributed single-circuit three-phase windings 30 electrical degrees apart. The double-wye winding with an external inter-phase transformer provides low ripple voltage to reduce filter size and also improves the winding utilization factor by forcing both windings to current share.

The stator is totally immersed in flowing Coolanol 25 through the slots and over the outer diameter in order to obtain direct cooling of the iron and the conductors. The coolant is contained by using a self-supporting carbon filament-wound tube in the stator bore (item 25), sealed at the ends by O-rings (items 99 and 100). Stator output ac electrical power is conducted from the stator using 12 hermetically sealed feed-through terminals bonded to the housing (shown on stator subassembly drawing).

The rotor assembly (Figure 3-4) develops the rotating field necessary for electrical energy generation in both the main and the auxiliary windings. The field is developed by high-energy rare earth-cobalt magnets mounted in a 12-pole configuration with tangential magnetic orientation. This construction permits the magnets to be supported in compression between flux focusing steel pole members to achieve maximum air gap flux density. This type of construction permits optimum utilization of all electromagnetic materials.

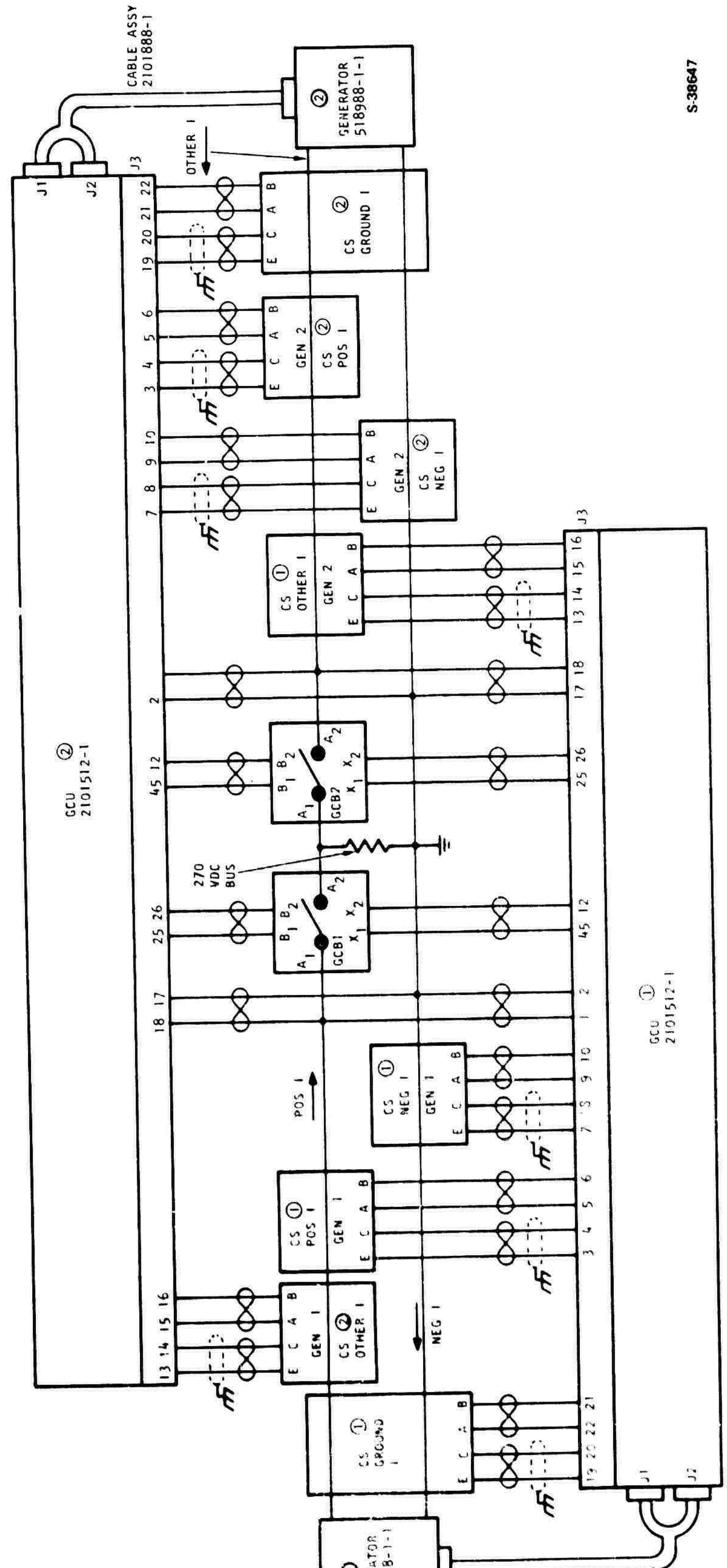


Figure 3-1. Interconnecting Diagram, 801577

The magnet operates at its maximum energy product, and air gap flux density is increased by the focusing effect of the pole members. Therefore the stator teeth are well saturated, and minimum length coils are needed to obtain the required flux linkage. Flexible, high-temperature epoxy is injected into the voids between the magnets and the rotor shaft-pole member assembly to assure magnet retention under all operating conditions. The rotor is encased in a thin Inconel 718 sleeve and thin Inconel end plates to protect the magnets on all sides.

The auxiliary stator is a separate generator excited by the rotor end leakage flux and provides electrically isolated control power and thyristor turn-on timing information. The stator stack consists of a tightly wound silicon steel strip core with a welded-on mounting ring. Two separate windings are installed in 36 slots. One winding is full-wave rectified internally to power the gate drive transformers; the other is mechanically phased with the main windings to provide voltage regulation information and electrical power to the GCU and also power to the external protection equipment.

Although both stators are excited by the same rotor, the magnetic paths are not the same. The magnetic circuits are such that when a high current fault condition exists on the main winding, the flux linking the auxiliary windings increases slightly. If control power were provided by an auxiliary winding in the main stator, then the magnetic paths would be common and voltage of the auxiliary power supply would be severely reduced by armature reaction effects of the main winding.

MECHANICAL DESIGN

The generator rotating assembly (Figure 3-4) is mounted on oil wick lubricated bearings with individual reservoirs and oil slingers. The method employed for bearing lubrication is depicted in Figure 3-5. As shown in the diagram, a cotton-packed oil-saturated sump contains two wicks which are in intimate contact with a rotating shaft. Capillary action through the wick carries oil from the sump to the point where the wicks embrace the shaft. At the shaft, centrifugal force directs the oil to an incline leading to the bearing. A centrifugal pump (shown to the right of the bearing in the diagram) forces the oil through the bearing where it is returned to the sump. In anticipation of flow in other than the preferred direction, a second centrifugal pump (shown to the left of the bearing) returns leakage oil to the sump. The pitot pump rotating cup assembly is cantilevered opposite to the output end, and the rotating group is axially preloaded by torquing the finger nuts to 90-100 ft-lb. The bearings are in steel inserts and preloaded from both ends by means of Belleville washers. This approach maintains preload on the bearings under all load conditions, thus minimizing bearing noise. Under balanced conditions, the bearing preload is approximately 60 lb on both bearings.

The quick-disconnect associated parts are shown on the output end; however, the activating mechanism has been removed from the generator due to test problems. The rotor is positioned by shimming to maintain an axial running clearance of 0.040 in. to the output end-bell hub, and 0.060 in. to the auxiliary stator and end-bell hub. The clearances are set up to prevent metal-to-metal contact of rotating and stationary parts under worst-case preload bottoming-out conditions.

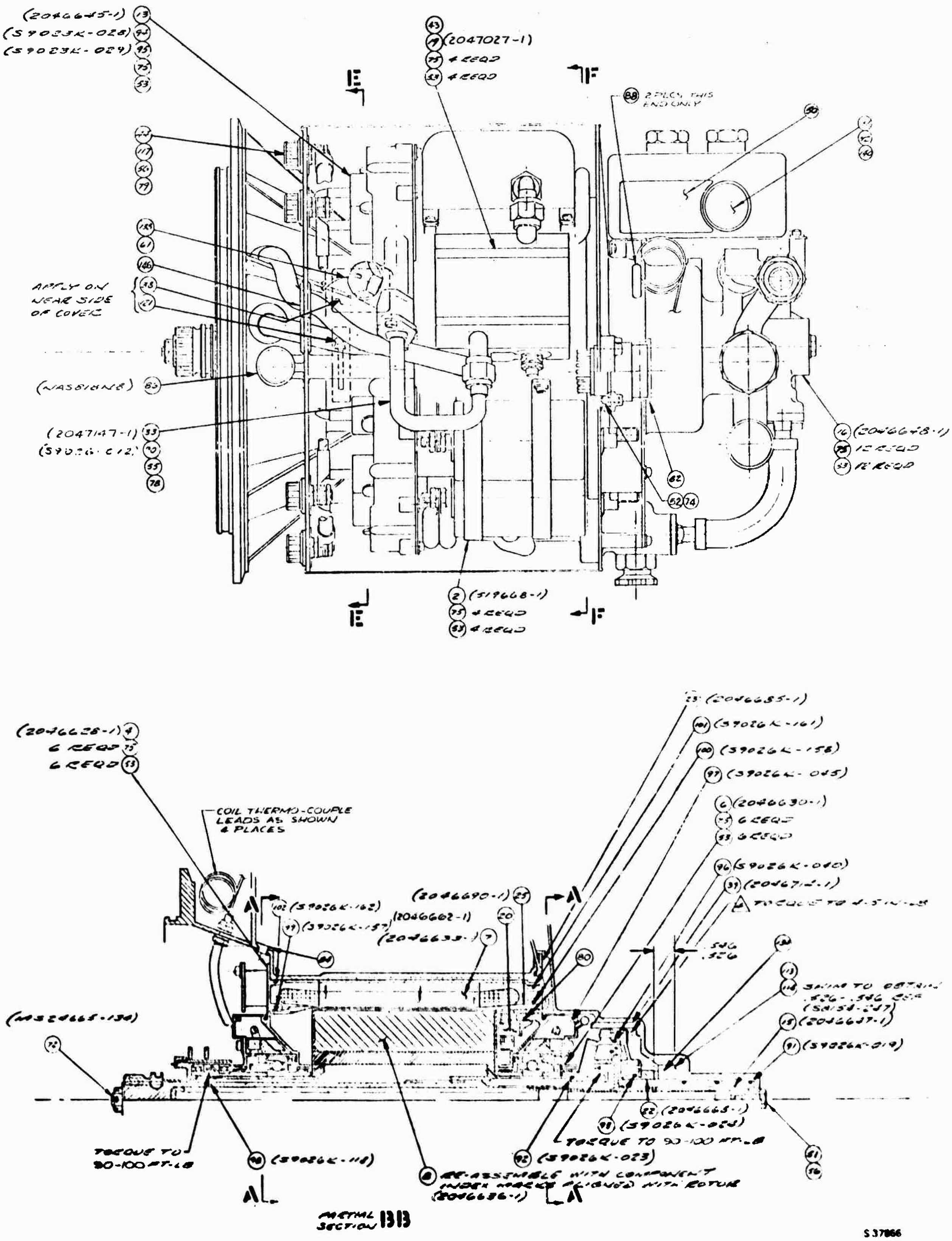


Figure 3-2. 270 VDC Generator Assembly, PN 518989-1 (Sheet 1)

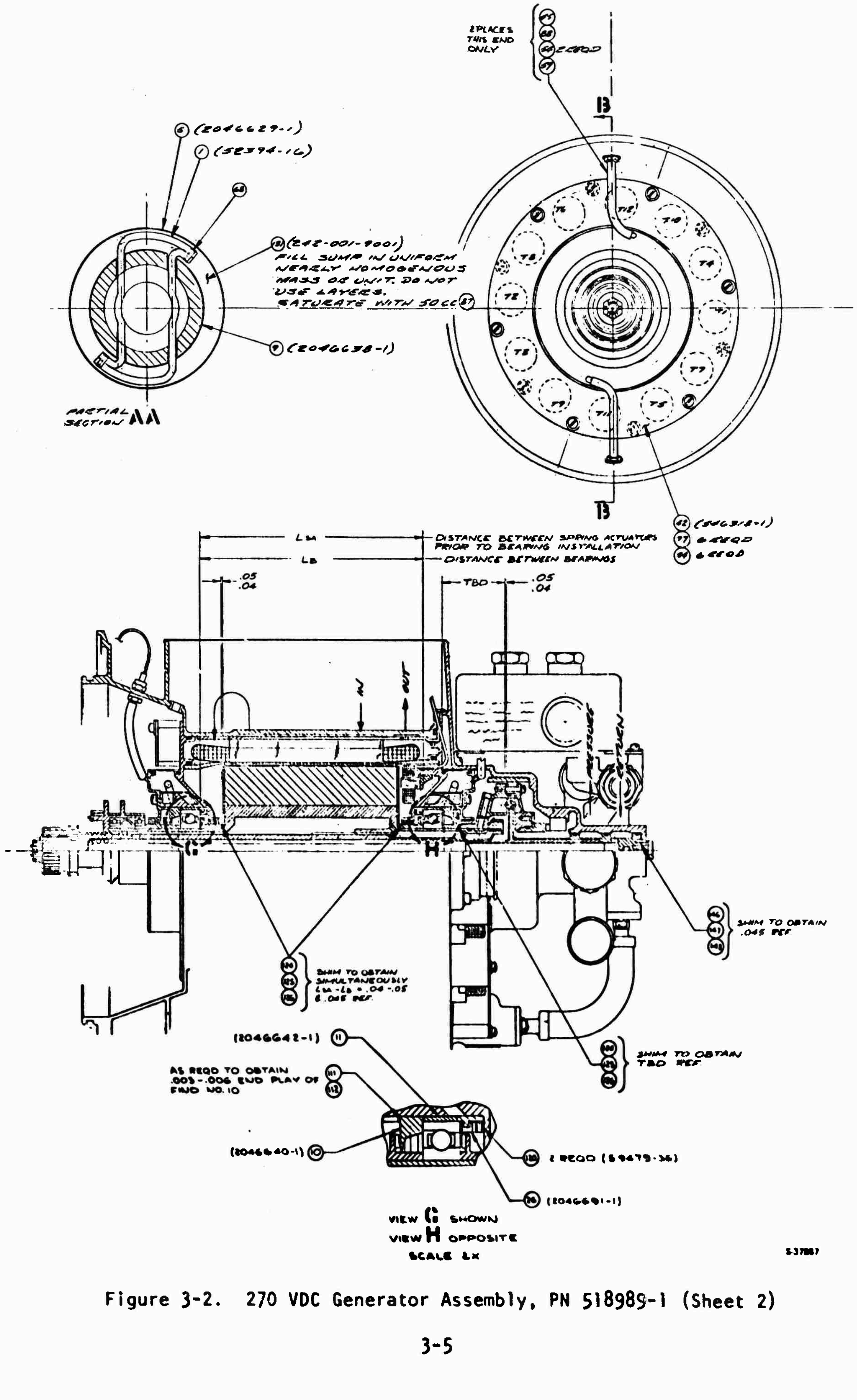


Figure 3-2. 270 VDC Generator Assembly, PN 518989-1 (Sheet 2)

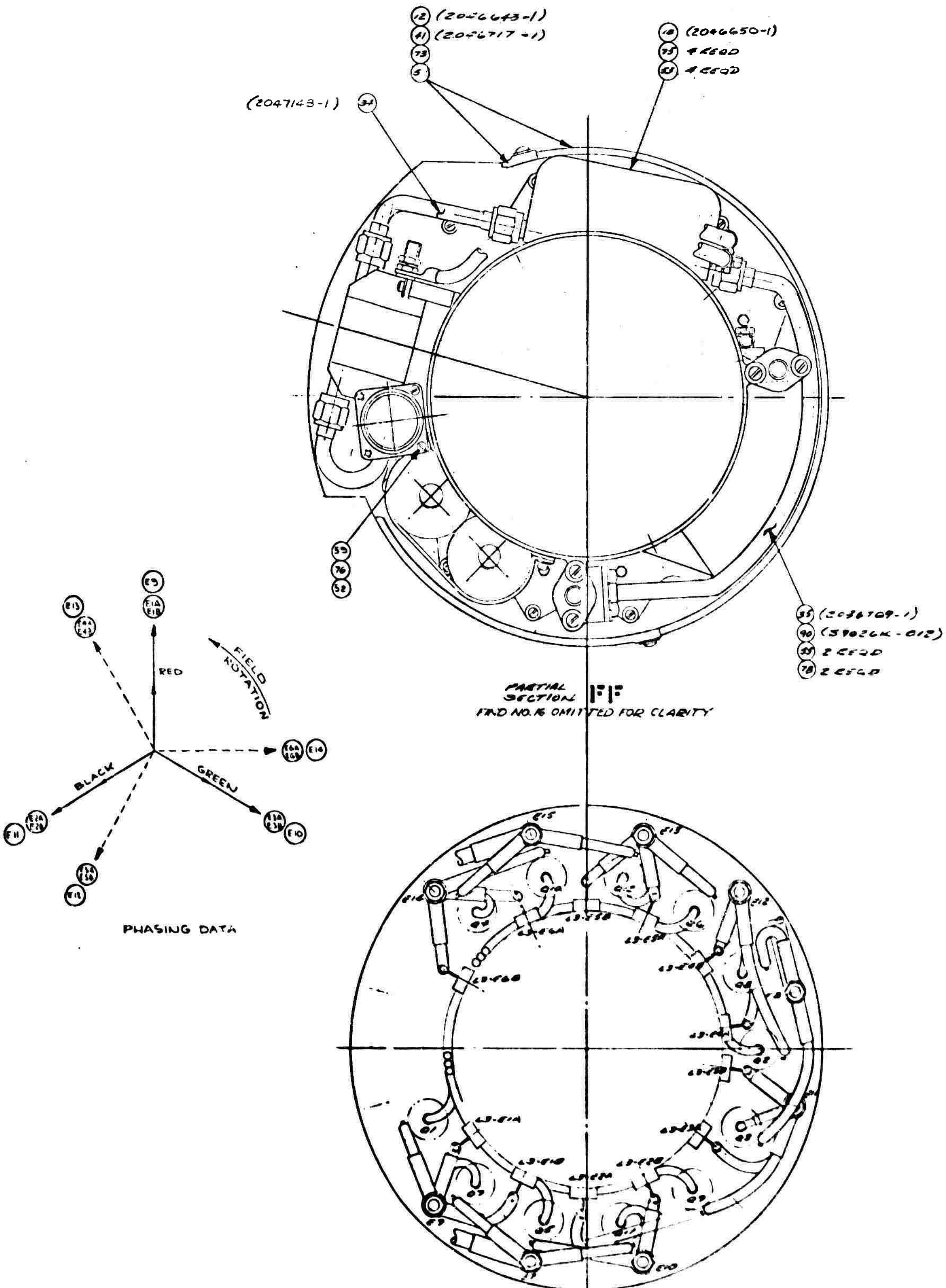


Figure 3-2. 270 VDC Generator Assembly, PN 518989-1 (Sheet 3)

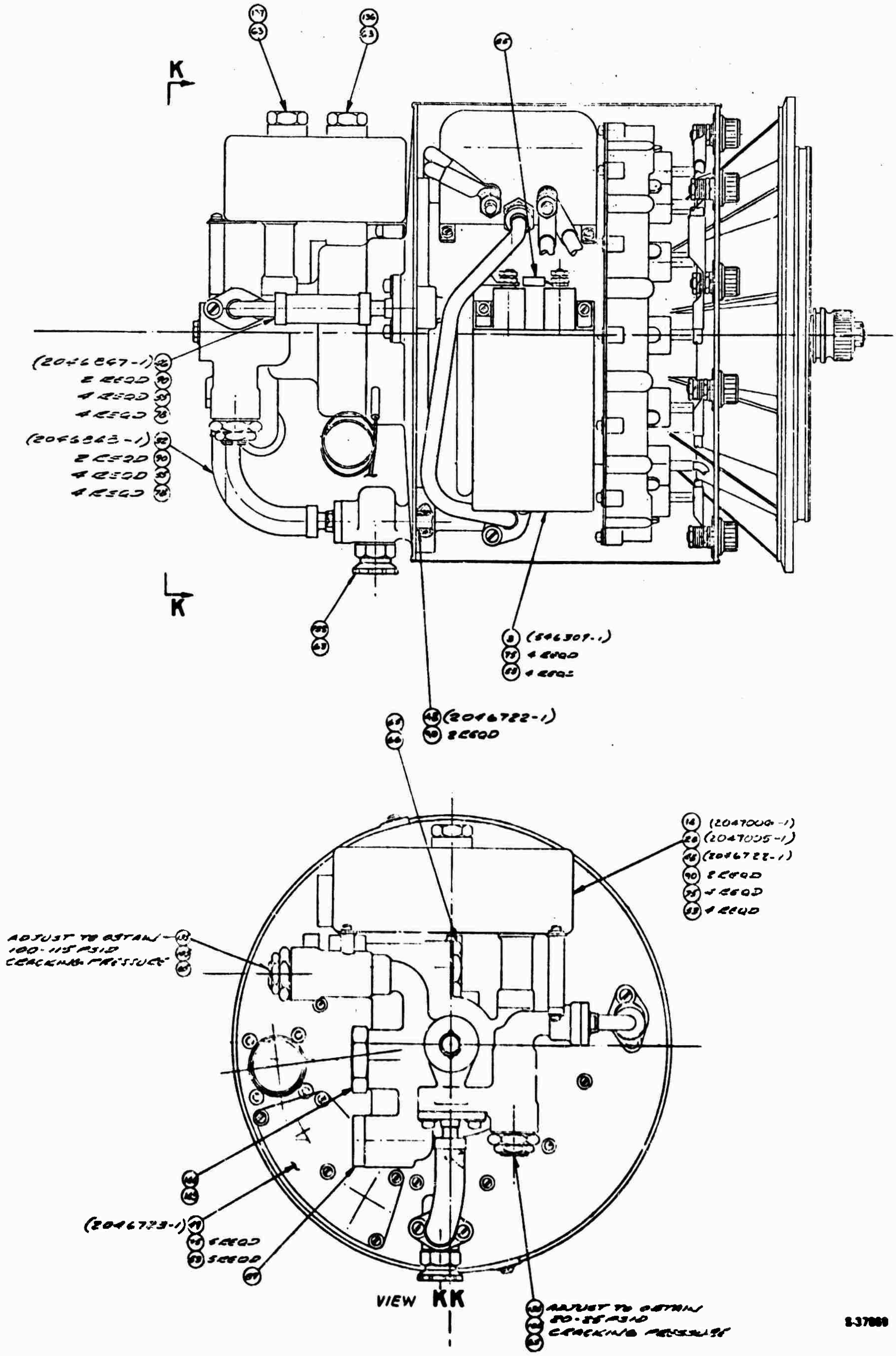


Figure 3-2. 270 VDC Generator Assembly, PN 518989-1 (Sheet 4)

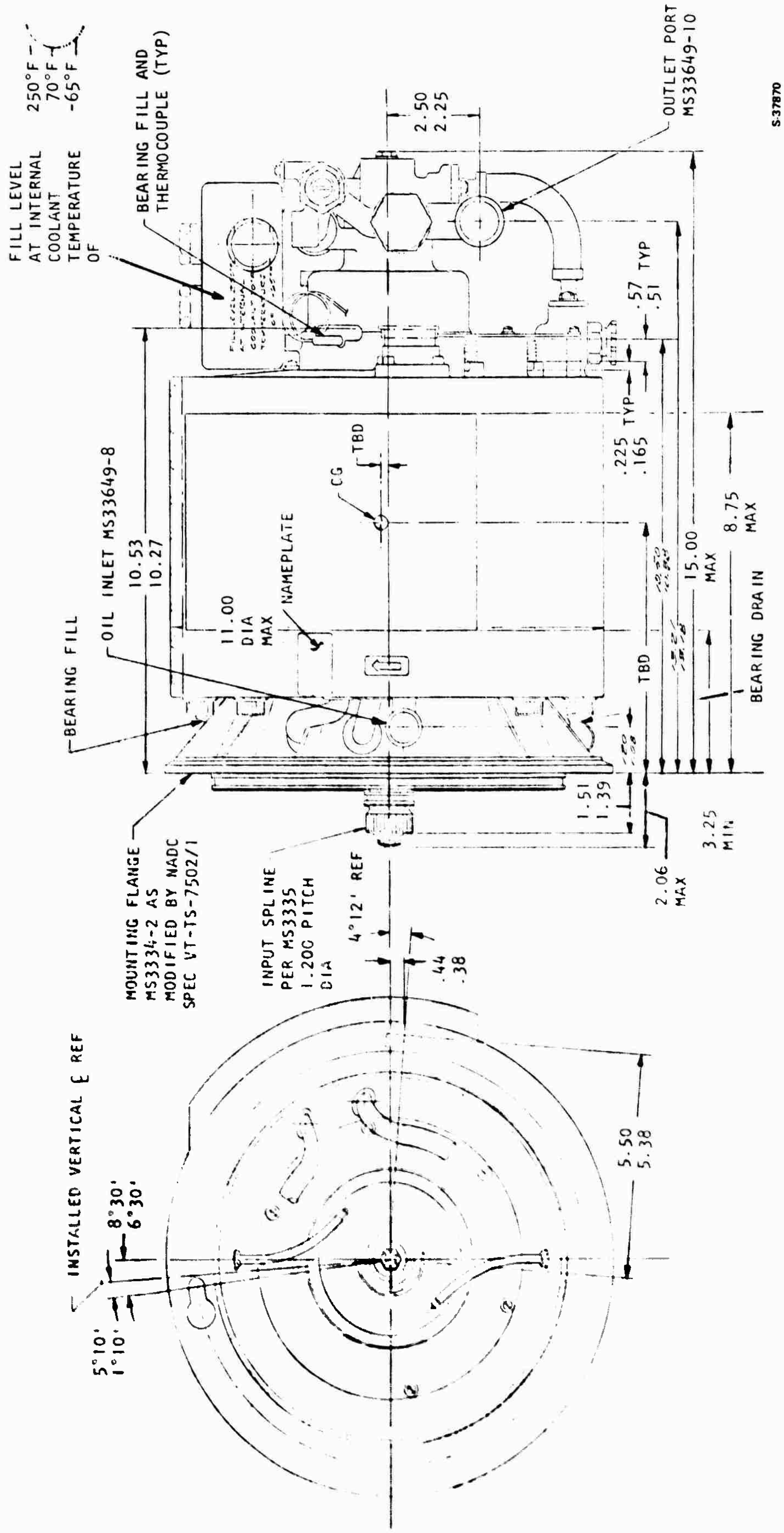


Figure 3-3. 270 VDC Generator Outline, PN 518988 (Sheet 1)

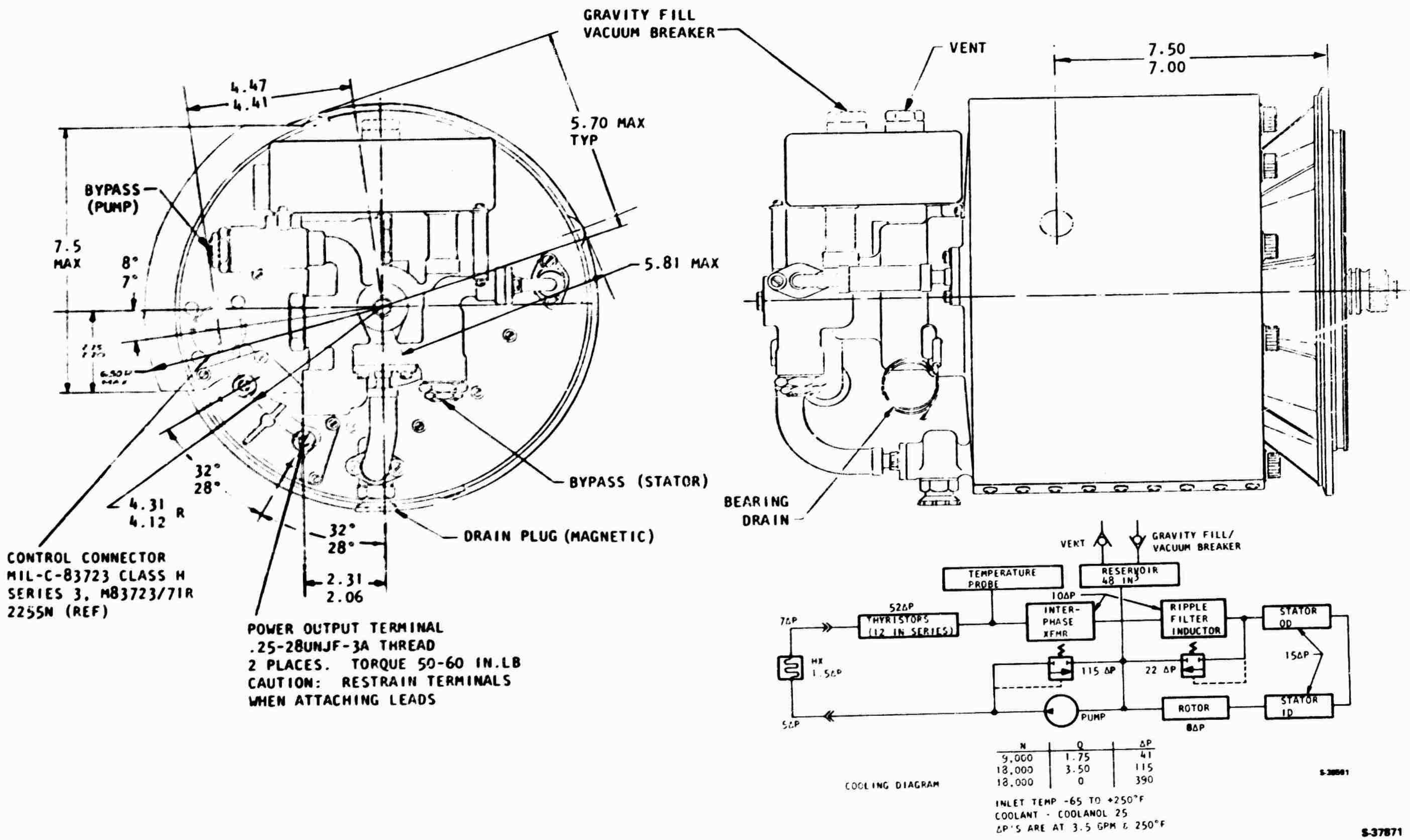
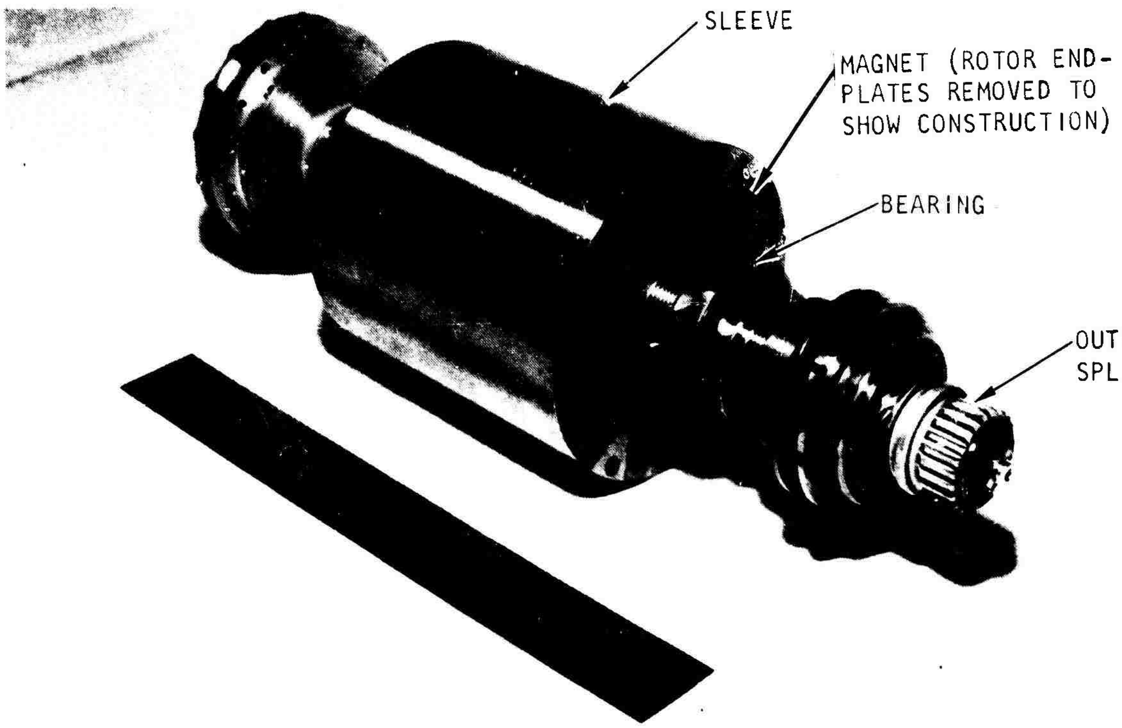


Figure 3-3. 270 VDC Generator Outline, PN 518988 (Sheet 2)



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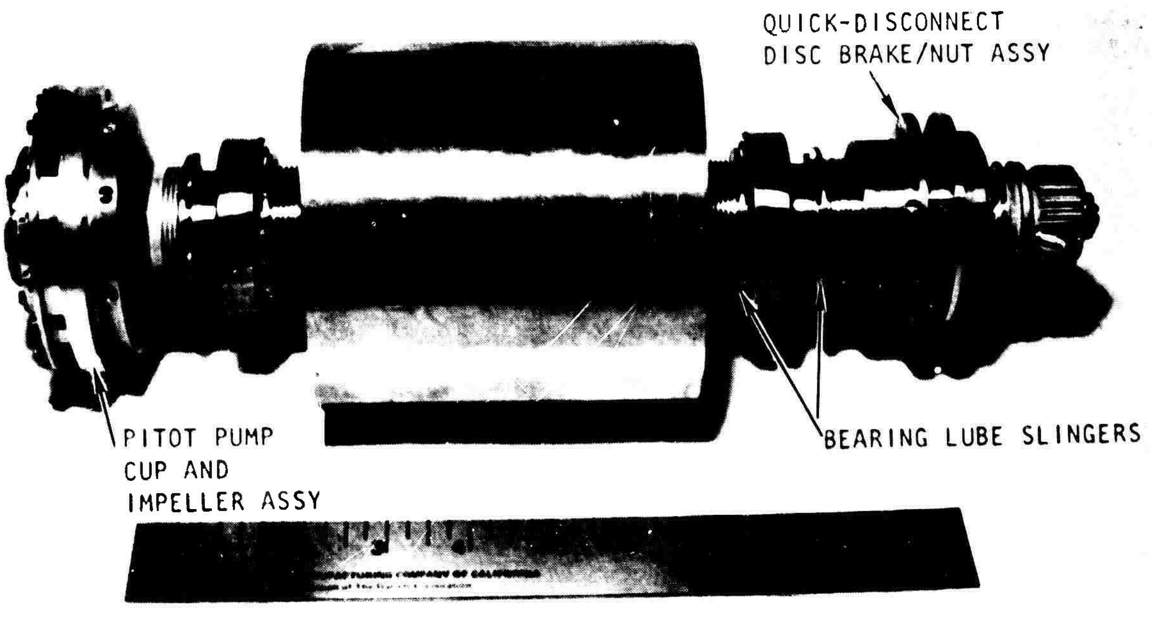

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Figure 5-4. Generator Rotor Assembly

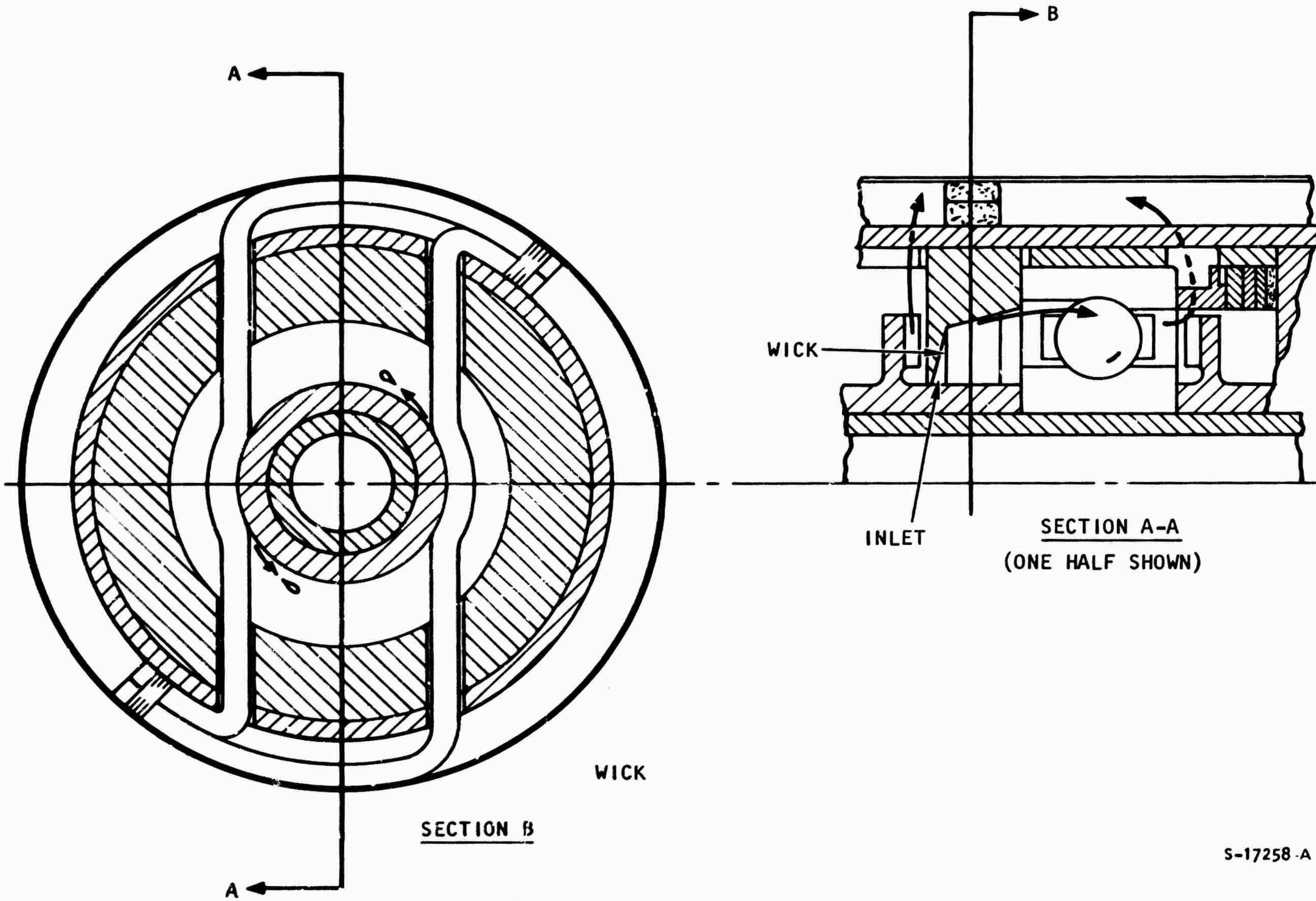

Figure 3-5. Wick-Lubricated Bearing Arrangement

The main housing assembly (Figure 3-6) provides support and alignment of the end bells and the rotating group with the stator and the pitot pump pickup tube assembly. Internally cast manifolding provides for proper coolant flow direction and distribution. Outside mounting provisions have been made for the ripple filter components and the interphase transformer. The gate drive transformer circuit board is mounted internally on the output end (Figure 3-7) with proper orientation of the gate drive transformers with their corresponding thyristors for close couplings.

The manifold assembly mounts on the rear end of the housing (Figure 3-8) and supports the reservoir (item 28 of Figure 3-2), relief valves (item 135), magnetic drain plug (item 133) and generator control unit cable connector. The generator assembly is enclosed in thin stainless steel covers (item 5) to provide mechanical protection and EMI shielding. Photographs of the complete generator assembly are shown in Figure 3-9.

THERMAL DESIGN

The generator assembly is liquid cooled with Coolanol 25 fluid as shown on the hydraulic schematic in the outline drawing, 518988 (Figure 3-3). Components cooled are the thyristors, main stator assembly, ripple filter inductor, interphase transformer and rotating group assembly.

A pitot pump (Figure 3-10) is used to develop the required pressure head and flow. Once the outer cup assembly starts to rotate, coolant is picked up by the stationary tube (Figure 3-2, item 15) and flow is directed through the cooling loop, starting with an external heat exchanger and filter. The thyristors are the most heat-sensitive elements in the assembly, therefore the coolest inlet oil is directed to these devices. The main stator and the other wire-wound components utilize a 220°C insulation system and they can be stressed to higher temperatures.

The completely submersed winding design is the most effective and practical means for cooling a compact, high-speed machine where heat concentration is high due to the high power rating achieved at small size. Utilization of a pitot pump makes the system self priming and insensitive to generator attitude.

The coolant is ducted through the assembly by means of integrally cast passages in the housing and the manifold castings, and external high-pressure tubing. Static sealing is achieved by the use of Coolanol-compatible O-rings and standard high-pressure hydraulic fittings. To reduce internal losses and simplify design, only one carbon face dynamic seal (item 134) is used. Coolant level can be monitored through the viewing glass located on the reservoir assembly (item 28). The photographs in Figure 3-11 highlight the manifolding, interconnecting, and fluid-level monitoring aspects of the design.

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Figure 3-6. Main Housing Assembly (Note Internal Fins)

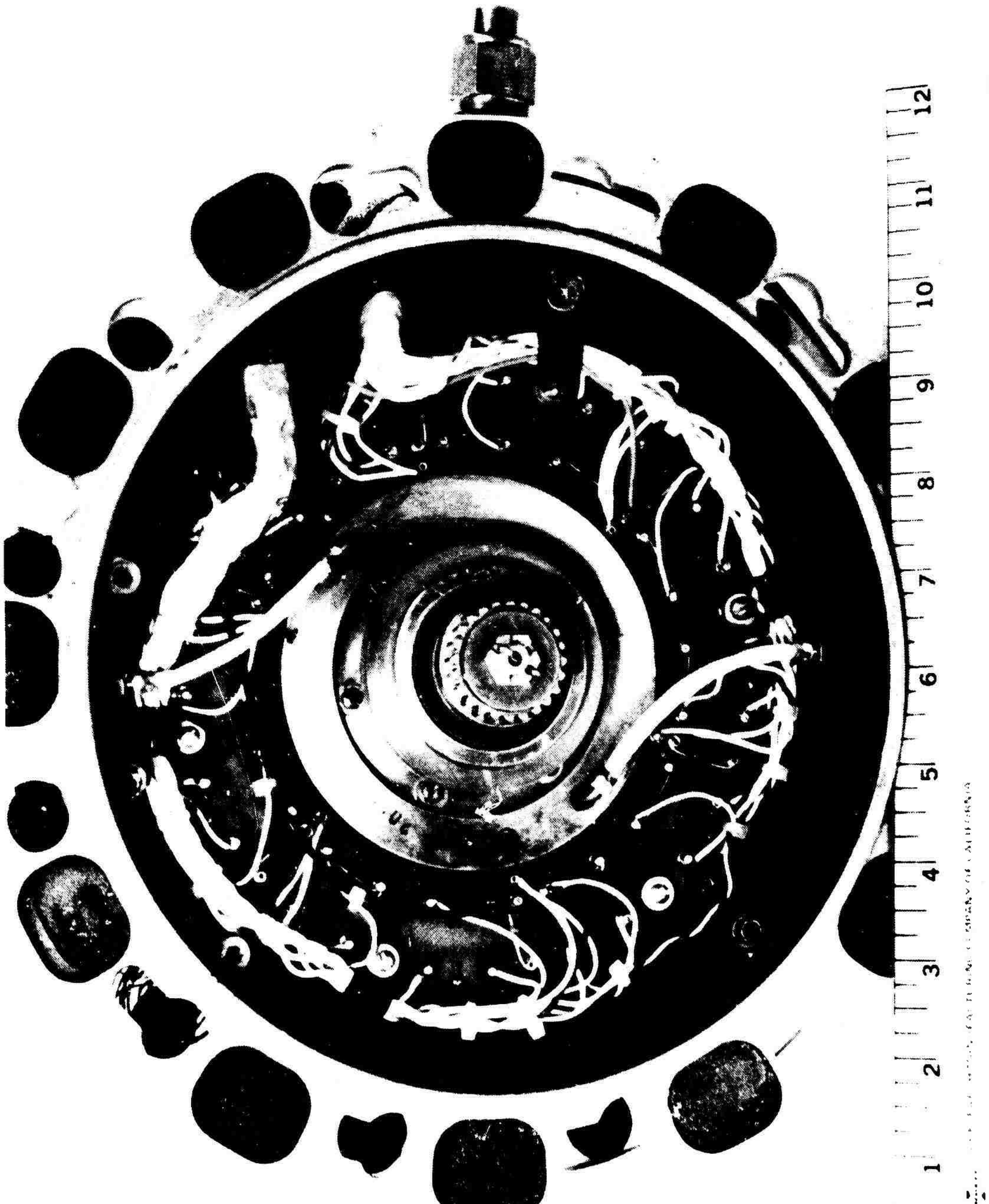

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Figure 3-7. Generator Output End, Showing Gate Drive Components

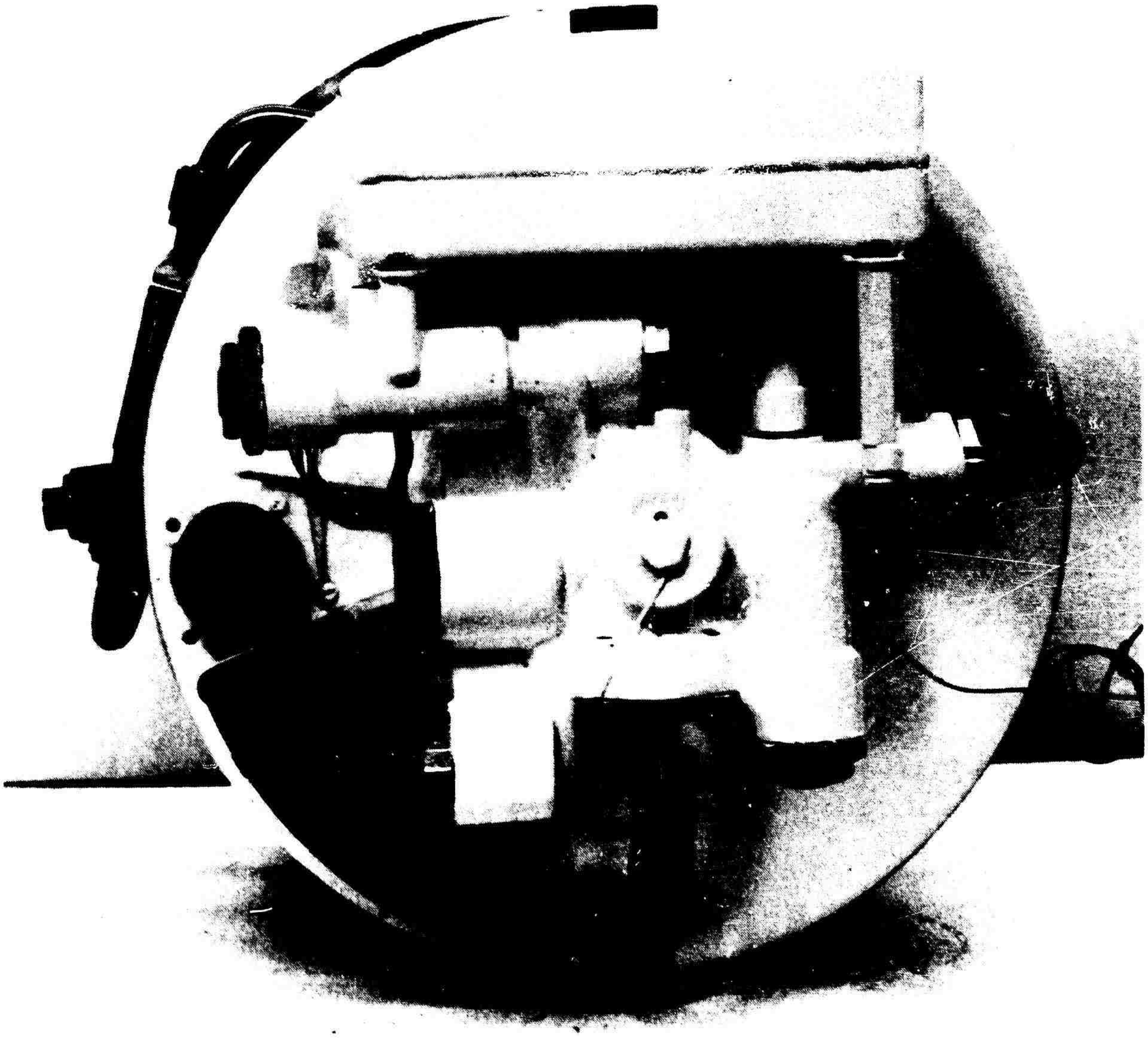

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Figure 3-8. Generator Rear End, Showing Manifold Assembly

F-30023

Figure 3-9. Complete Generator Assembly

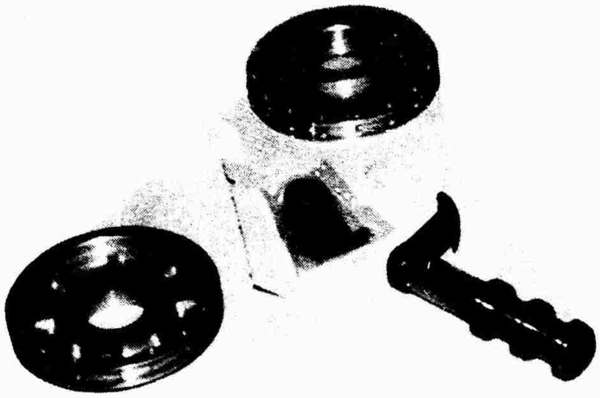
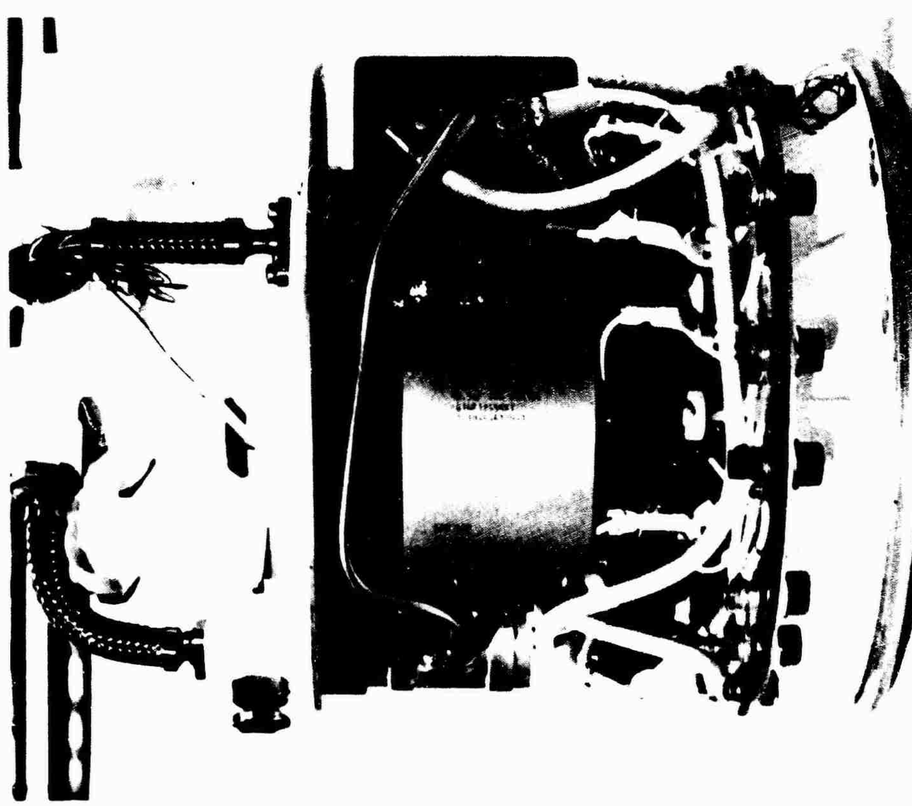


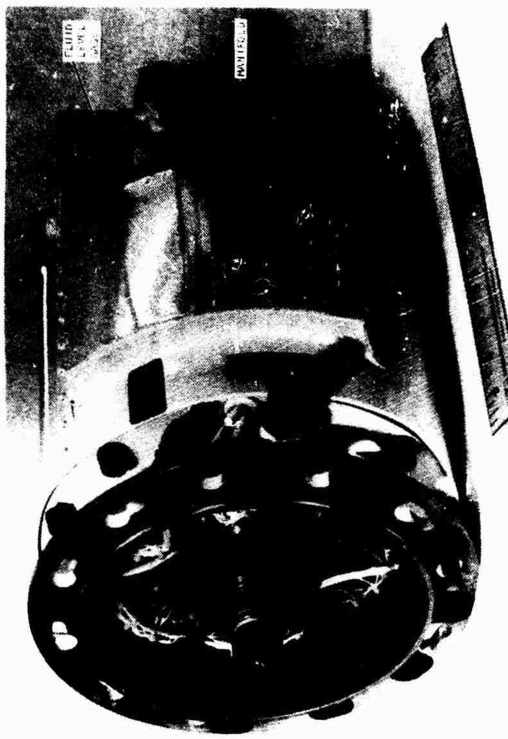
Figure 3-10. Pitot Pump

The interphase transformer method of paralleling the two phase-controlled rectifiers forces the current in both bridges to be equal. The maximum average steady-state current in each thyristor is 41.7 amperes. This causes 38 watts of maximum steady-state power dissipation in each thyristor. This power is removed via an aluminum pin fin-to-oil heat exchanger.

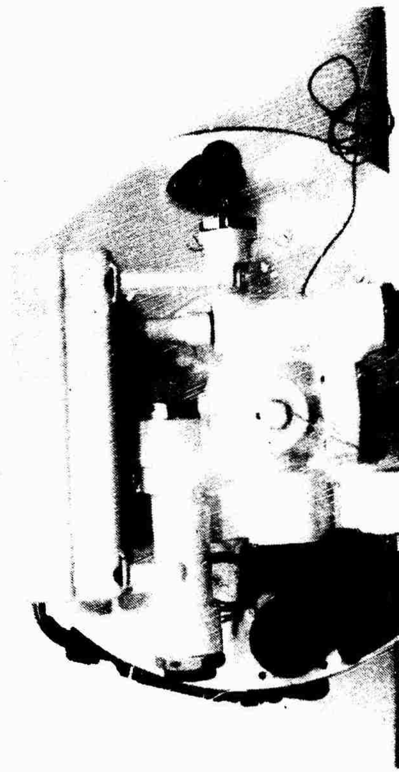
The phase-controlled rectifier accomplishes voltage regulation by modulating the conduction angles of the thyristors. This phase-controlled rectifier configuration has bilateral capability. It can actively increase as well as decrease the output voltage of the power converter. When the delay angle of the phase-controlled rectifier exceeds 90 electrical degees, power is returned to the alternator. The 12-pulse operation, combined with the 900-Hz minimum alternator frequency, causes the phase-controlled rectifier to have a minimum bandwidth of 2.7 kHz. This type of modulation produces more output ripple voltage than a diode rectifier at all conduction angles except "full on."



FLUID INTERCONNECTING LINES AND COOLING



CABLING, FLUID LEVEL GAUGE, AND MANIFOLD



MANIFOLD ASSEMBLY

F-30022

Figure 3-11. Generator Design Aspects

POWER CONVERTER

GENERAL DESCRIPTION

The power converter changes the variable ac power from the permanent-magnet generator to constant voltage (270 vdc) power. The circuit chosen for this function is a 12-pulse phase-controlled rectifier. The block diagram of this power converter is shown in Figure 3-12. The permanent-magnet machine generates variable voltage and variable frequency ac power. This power is supplied to the power converter in two three-phase groups. Thirty electrical degrees of displacement are between the two three-phase groups. The variable ac power from each three-phase group is rectified and regulated by the respective three-phase phase-controlled rectifiers.

The dual three-phase rectifier approach was chosen because it reduces the thyristor currents to levels that are compatible with the available cooling scheme. The output current divides equally between the two three-phase rectifiers.

The control of the phase-controlled rectifiers originates in the GCU, using phasing information from the auxiliary stator. Control functions include voltage regulation and fault current limiting. The control signals from the GCU are received by the gate driver block, amplified, and transmitted to the phase-controlled rectifiers.

The outputs of the two phase-controlled rectifiers are combined in the interphase transformer. The interphase transformer forces the currents in the two phase-controlled rectifiers to be equal and reduces the amplitude of the ripple voltage to one-half of the value for a single phase-controlled rectifier.

The ripple filter attenuates the ripple at the output of the interphase transformer to the required level.

DETAILED DESCRIPTION

Figure 3-13 is a schematic diagram of the power electronics phase-controlled rectifiers. The phase-controlled rectifiers are full-wave, three-phase, thyristor bridges. The input to each bridge is variable three-phase power from the PM generator ranging from 207 volts L-L at 900 Hz to 455 volts L-L at 1980 Hz, which covers the maximum speed for regulation.

International Rectifier 81 RLA thyristors were chosen for the phase-controlled bridges. These thyristors have a maximum rated junction operating temperature of 150°C. This allows cooling by 120°C oil. Most thyristors are rated for 125°C maximum operating junction temperature, which cannot be cooled by 120°C oil. The selected thyristors have a blocking and reverse voltage rating of 1200 volts. In this application, the maximum voltage experienced by any thyristor is 575 volts. This degree of voltage derating enhances the operational reliability of the thyristors. The operational reliability of the thyristor is further improved by the AiResearch 72-hour blocking life testing for each thyristor at 150°C junction temperature and 1200 vdc forward blocking voltage.

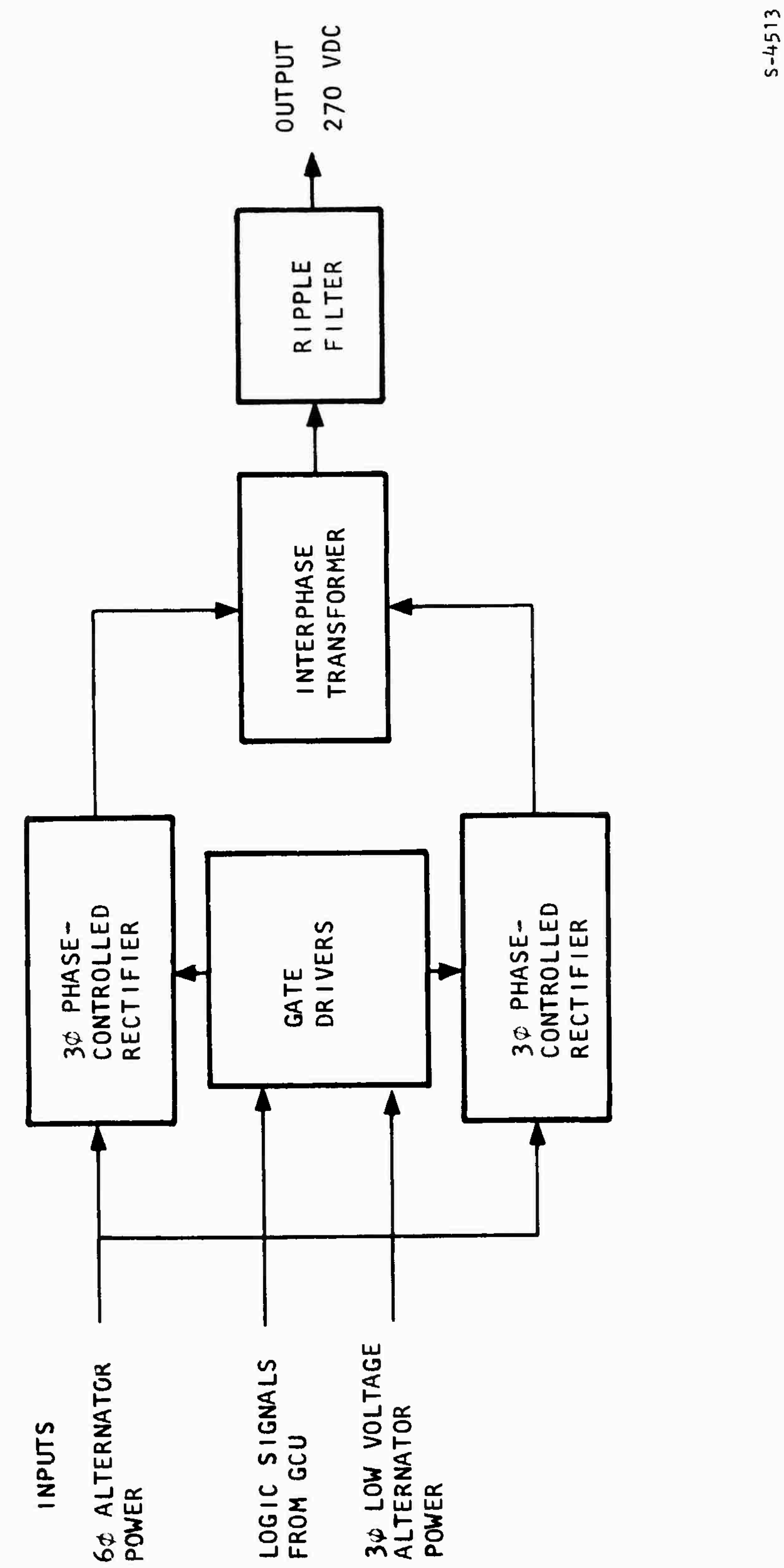


Figure 3-12. Block Diagram, Power Converter

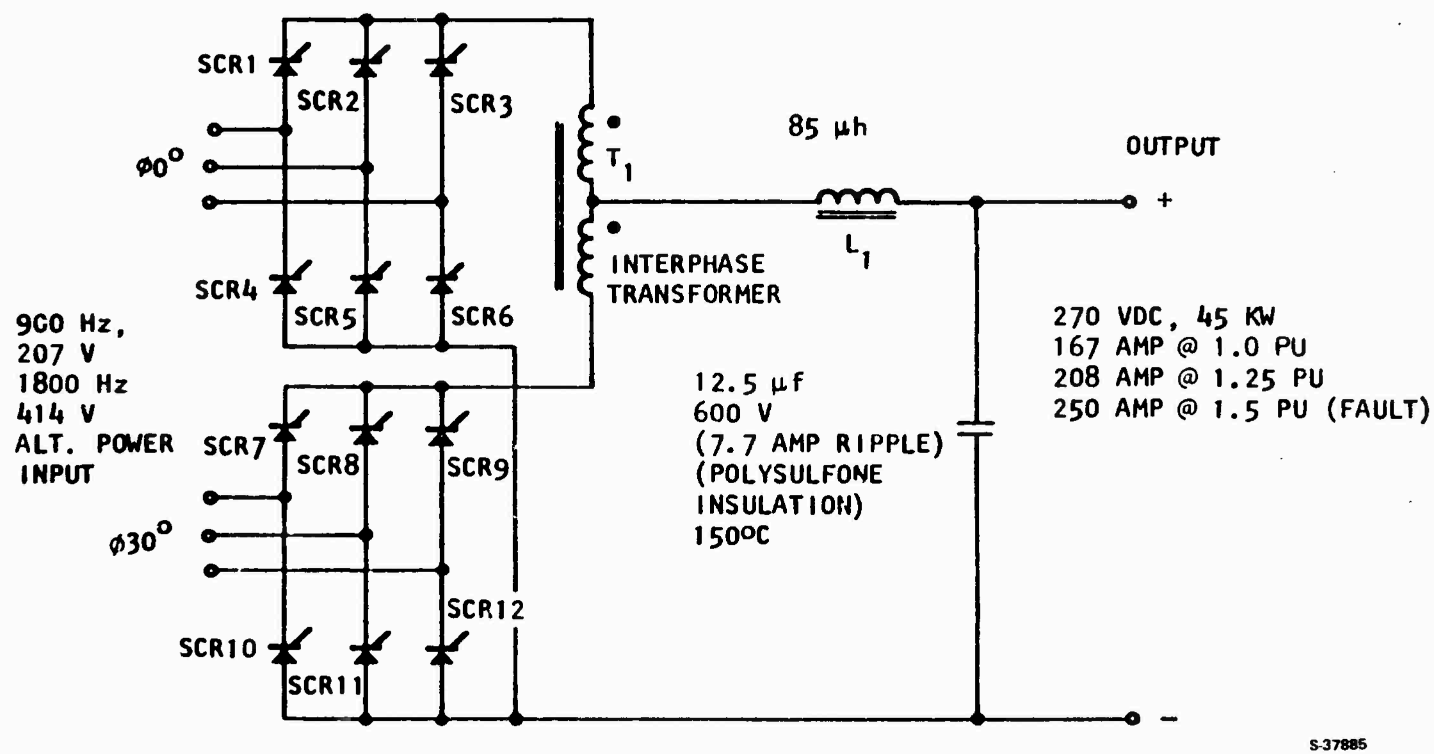


Figure 3-13. Schematic Diagram, NADC 270-Volt Power Converter, Power Electronics

Figure 3-14 shows the output voltage waveform of one phase-controlled rectifier at the maximum required delay angle, which also produces the worst-case ripple voltage. The other phase-controlled rectifier produces a similar waveform displaced 30 electrical degrees from the waveform of Figure 3-14. The paralleling of the two phase-controlled rectifiers by the interphase transformer not only forces current sharing, but reduces the ripple voltage to the waveform shown in Figure 3-15. Note that the ripple frequency has also been increased to 12 times the generator frequency.

The losses associated with the phase-controlled rectifiers are estimated to be 456 watts. This represents 60 percent of the total power converter losses. The total power converter efficiency is estimated to be 98 percent.

INTERPHASE TRANSFORMER

The interphase transformer is a three-terminal device that forces the dc load current to divide equally between the two phase-controlled rectifiers and reduces the rectifier ripple voltage. The interphase transformer is wound on a C-core to minimize size and weight. The transformer dissipates 250 watts at the maximum rated load conditions. This dissipation is removed by the coolant flowing through the transformer assembly.

RIPPLE FILTER

The ripple filter is a low-pass L-C network consisting of an 85-μh inductor and a 12.5-μf capacitor. The filter inductor is wound on a gapped C-core. The inductor weighs 1.2 pounds and dissipates 88 watts at full-rated, steady-state load. It is designed to remain unsaturated up to 1.25 per unit load current. The inductance is sized to prevent discontinuous current in the phase-controlled rectifier down to 0.1 per unit load. The filter capacitor is an extended foil, polysulfone structure that is rated for 150°C operation. The ripple current in the filter capacitor is 7.2 amp at 21.6 kHz. Polysulfone was chosen for its excellent operating temperature range (-65° to 150°C). The filter capacitor weighs 0.6 pound and dissipates less than 5 watts.

CONTROL ELECTRONICS

The control electronics, shown in block diagram form in Figure 3-16, controls the 270 vdc output of the phase delay rectifier over the full speed range of the generator and 0 to 150 percent of full load. Another feature of the controls is to sense fault conditions within the generating system and shut the system down when it is not performing within certain specified limits.

Figure 3-17 is a block diagram of the voltage regulator. Voltage regulation is achieved by controlling the firing angle of the silicon-controlled rectifiers (SCR) in the phase-delayed rectifier (PDR).

In order to synchronize the SCR gate firing with the generator sinusoidal voltage output, a sync waveform is received from an auxiliary winding on the generator. The sync waveform is first integrated to remove noise which may be fed back from the main generator windings; it is then compared with the voltage regulator error signal α.

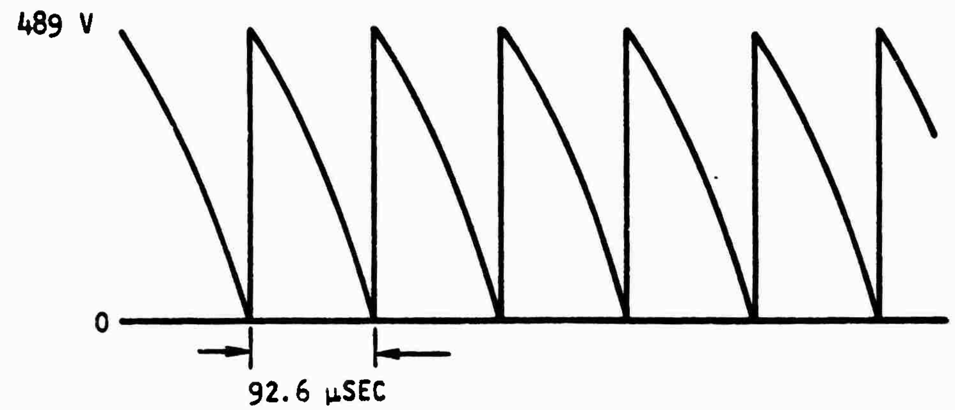


Figure 3-14. Phase-Controlled Rectifier Ripple Voltage for 60-Degree Delay

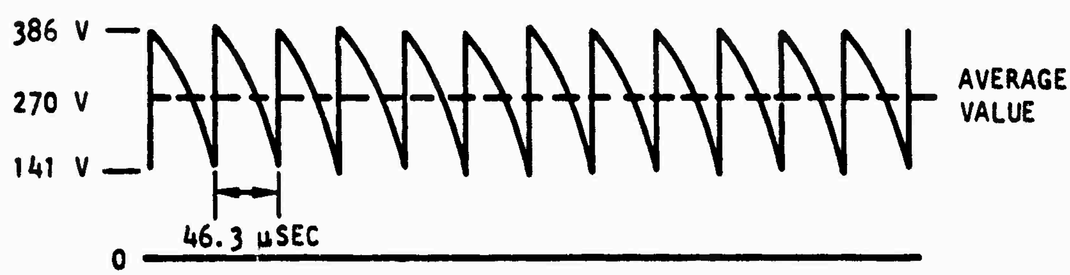


Figure 3-15. Interphase Transformer Output Ripple Voltage

S-37887

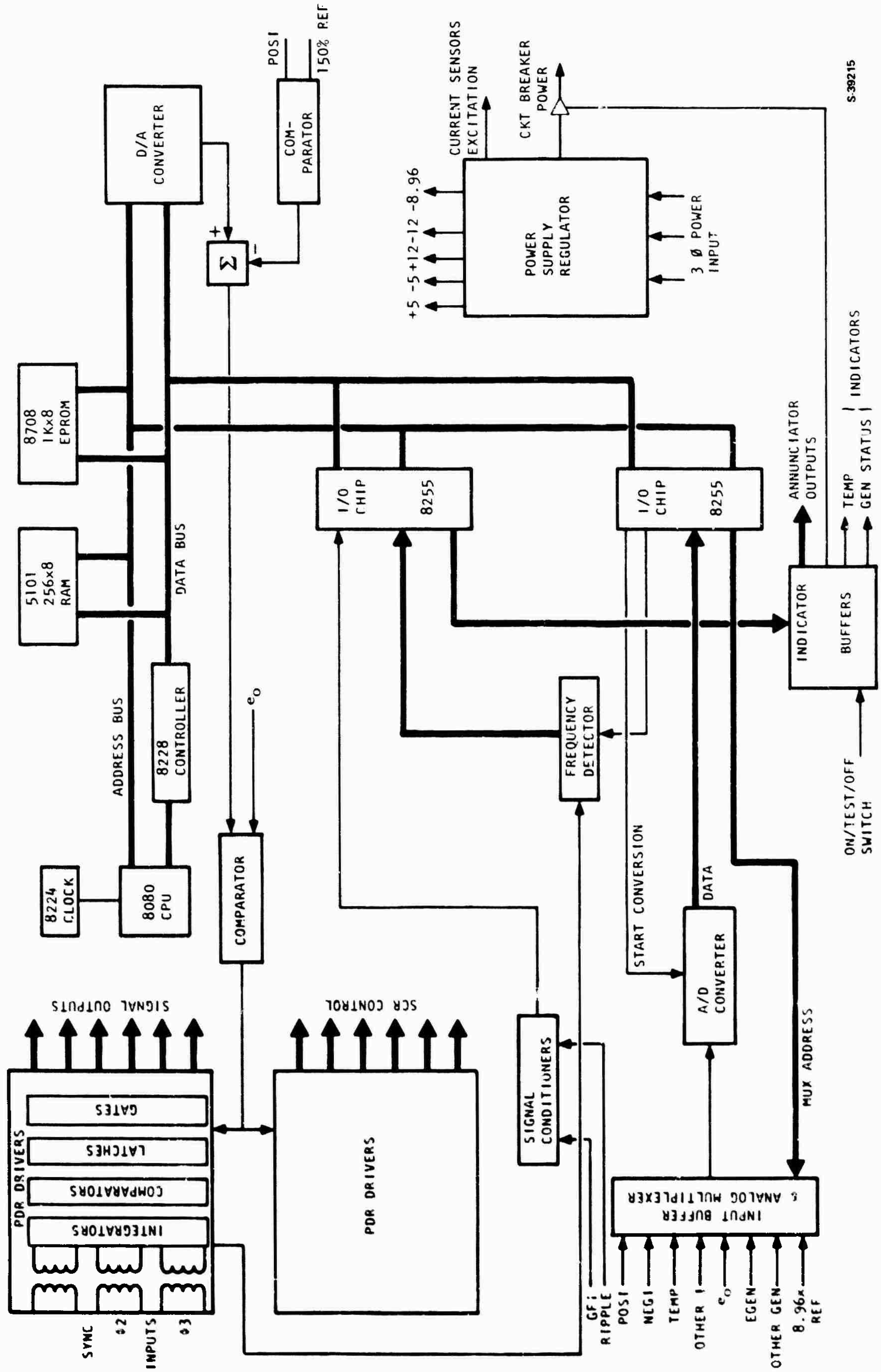


Figure 3-16. GCU Block Diagram

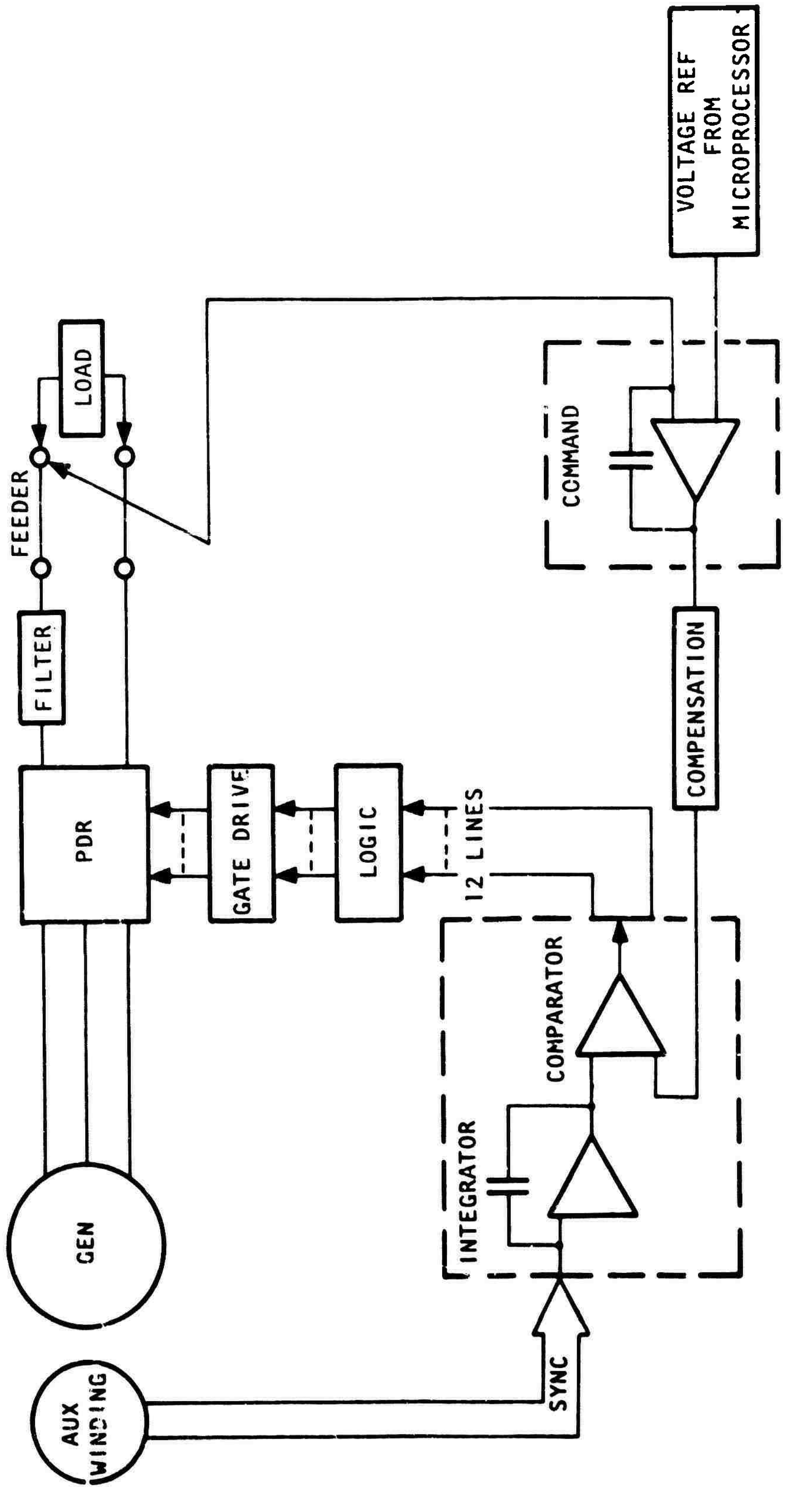


Figure 3-17. Block Diagram, Voltage Regulator

The comparator section, which is discussed in detail later, produces pulses of fixed width which can be varied in phase relationship with the generator sync waveforms. Thus by changing the command it is possible to change the phasing of the comparator output in relation to the sync waveforms.

The comparator outputs are then fed to the logic block which produces synchronized pulses of varying pulse width to drive the gate drive circuitry.

The command block senses the voltage at the point of regulation and compares it to the 270 vdc reference generated by the microprocessor. After an integration the command is fed into the comparator to control the PDR firing angle and hence the 270 vdc line voltage. Dynamic compensation has also been added to the forward control loop to optimize response to load and speed changes.

The package consists of the following:

Two PDR control boards

One voltage regulator board and I/O

One microprocessor and memory board

One power supply

The two PDR boards are identical and each contains the circuitry to control six SCRs. Each control lane consists of the following:

Sync line transformer

Sync integrator

α command limit

Comparators (2)

Logic

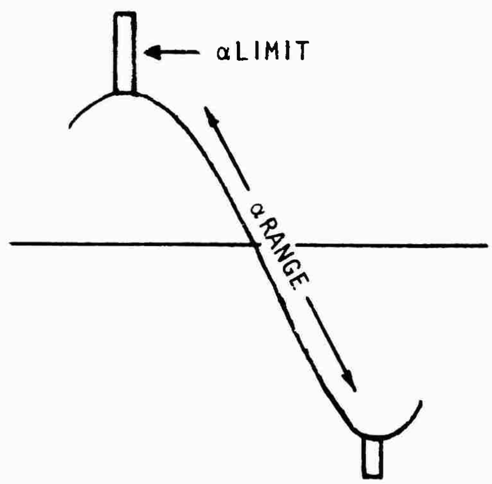
SCR transformer drive circuit

The sync line transformer isolates the sync circuitry and also produces the necessary phase shift from the three-phase auxiliary winding output. One set of three transformers is connected line-to-line and the second set line-to-neutral to produce six waveforms of 20-degree phase displacement. A poteniometer is provided across each transformer to set the integrator output. This potentiometer may also be used in setting up the PDR firing for minimum ripple. With reference to the circuit diagrams, these transformers are T_1, T_2, T_3 (see Figure 4-22).

The sync line integrator is a low offset amplifier and is sealed to produce a 12V p-p output waveform. Since the machine output has a constant volts/Hz ratio, the integrated sync waveforms are always a constant amplitude and independent of generator speed.

The α command limit amplifier looks at the two remaining sync lines; i.e., if the AØ waveform is being integrated, BØ and CØ are compared for equal voltage which occurs when AØ is at positive peak and BØ and CØ are negative but equal.

At the BØ and CØ crossing point of the α limit comparator switches, this output is differentiated and added to the integrated output of phase A to cause a "blip" to be formed on the waveform as shown in the following sketch.



This "blip" on the waveform has a magnitude equal to 15 volts. This circuit now limits the range of α to 180 degrees and ensures that the PDR is always in the correct quadrant of operation.

The high-speed comparators form the logic pulse train by comparing the dc level of the α command with the sinusoidal integrated sync line. A positive and negative comparison is made, producing two pulses of 180-degree phase displacement and with the ability to be adjusted by the α command over a range of 180 degrees. The negative-going edges of the two comparator outputs are used to operate a latch whose output will thus be a square wave with a phase determined by the instant the α comparator switched negative. For a detailed explanation and timing diagrams see the "PDR logic" part of the "Analytical Evaluation" section of this report. Since there are three phases, there will be three square waves and their complements. A series of logic gating produces the SCR gate drive waveforms which are a string of twelve pulses evenly spaced at 30 degrees from each other.

SCR Transistor Drive Circuit

The SCR drive transformers and power supply are located in the generator housing. The transformer is designed such that it requires a 2:1 duty cycle on the primary. The primary drive circuit is designed to accommodate this requirement. The 160-ohm and 640-ohm resistors are to protect the drive stage should the transformer primary saturate. The transistors in the primary circuit are driven from TTL logic.

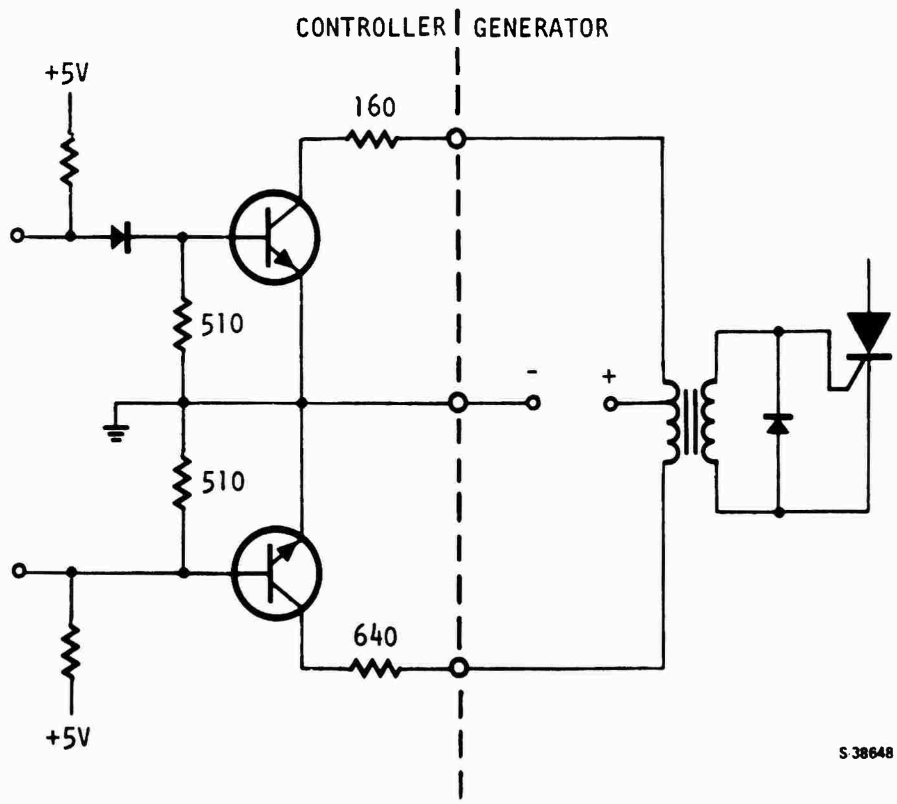


Figure 3-18. SCR Transformer Drive Circuit

Computer Operation

The GCU (generator control unit) uses an 8080 microprocessor to monitor the operation of the generator; 1K of EPROM is used to store the program, and 256 bytes of CMOS RAM are used for scratchpad. Two 8255 peripheral chips provide 48 input/output lines.

The microprocessor generates a reference voltage through a D/A converter which determines the output voltage of the generator. The regulation of the voltage is implemented in hardware. The microprocessor also provides an SCR ENABLE discrete output which will either enable or disable the firing of the SCR. When the generator is building up in speed, the SCRs are disabled until the speed reaches 9000 rpm. The SCRs are then enabled and the reference voltage is ramped from 0 volt to 5.13 volts, which will produce a 270-volt output at the generator. The ramp time is approximately 150 msec.

Once the generator is running, the microprocessor will enter a 10 msec loop where it will monitor different parameters of the generator to determine if a fault condition exists. If there is a fault, the microprocessor will shut down the generator by first ramping down the reference voltage to 0 volts and then disabling the SCRs and opening the generator line contactor (CLC). The different fault conditions are overload, overvoltage, undervoltage, underspeed, feeder fault, excessive ground current, and excessive ripple. These faults are described in greater detail in the "270V GCU Software" discussion. As can be seen from Figure 3-16, the microprocessor can select one of several analog channels, start the A/D conversion, wait for the end of conversion and read the A/D output.

SECTION 4

ANALYTICAL EVALUATION

Extensive analytical work was done in the critical design areas to assure system performance. The following paragraphs summarize the work relating to the final design.

STRESS AND CRITICAL SPEED ANALYSES

Static and dynamic stress analyses were conducted for the 270 vdc permanent-magnet generator, PN 518988. The main loads concerned in the analyses are presented in Table 4-1. The calculations are shown in Figures 4-1, 4-2 and 4-3.

Figure 4-1 shows a cross-section of the generator assembly and tabulates materials, critical loadings, applied stresses, allowable stresses and margins of safety for critical components. A shaft-shear torque of 5,000 inch-pounds and a 1,000-pound pulse force were used as the critical design loads for the driving shaft and the nut coupling.

Based on the stated loads, all components of the permanent-magnet generator assembly have positive margins of safety. Therefore, the generator assembly is considered acceptable from the viewpoint of structural integrity.

In addition to the stress analysis, the generator rotor was also subjected to dynamic analysis in searching rotor critical speed as well as system natural frequencies. For the rotor alone, supported on ball bearings with an equivalent spring rate of 910,000 pound/inch at each end, the lowest critical speed is 34,770 rpm. Figure 4-2 shows the mode shapes of the first and second critical speeds of the rotor. Since the pump assembly will be cantilevered at one end, flexibilities of the assembly component structure can logically reduce the magnitude of the lowest critical speed (natural frequency).

A refined dynamic model which simulates mass and stiffness of the entire generator structures including the aluminum housing, the steel stator sleeve, bearing housings and ball bearings, was established to evaluate the system natural frequencies. The lowest natural frequency was found at 400 Hz (24,000 rpm). Figure 4-3 represents lateral harmonic responses at both ball bearing locations for frequency ranges up to 1200 Hz. The input lateral force excitation along the rotor length was 17 pounds total. Amplification factors were estimated as 1.5 and 3.5 for the generator operating at the maximum speed of 18,000 rpm and at the 20 percent overspeed of 21,600 rpm respectively.

TABLE 4-1. MAIN LOADS CONCERNED IN STRESS ANALYSIS

(a) Acceleration (1) Non-operating during test, operational after test a = 135.5 g (2) Operating during test, operational after test a = 9.0 g
(b) Shock (1) Non-operating during test, operational after test 15 g, 11 msec, half sine pulse (2) Crash; 30 g, 11 msec, half sine pulse Non-operational after test; no parts came loose
(c) Vibration MIL-STD-810B, Figure 514.1-1, Curves AT and Z Input at resonant frequency = 10 g Response to input = 100 g (assumed amplification factor of 10)
(d) Cooling Oil Pressure Oil pressure varies at different locations 115 psig peak pressure is assumed in operating
(e) Rotating Speeds (1) Normal maximum operating speed 18,000 rpm for the life of 10,000 hours (assumed a total of 10,000 cycles with the maximum rotor temperature of 315°F) (2) 120% speed 21,600 rpm for 5 minutes (one cycle)

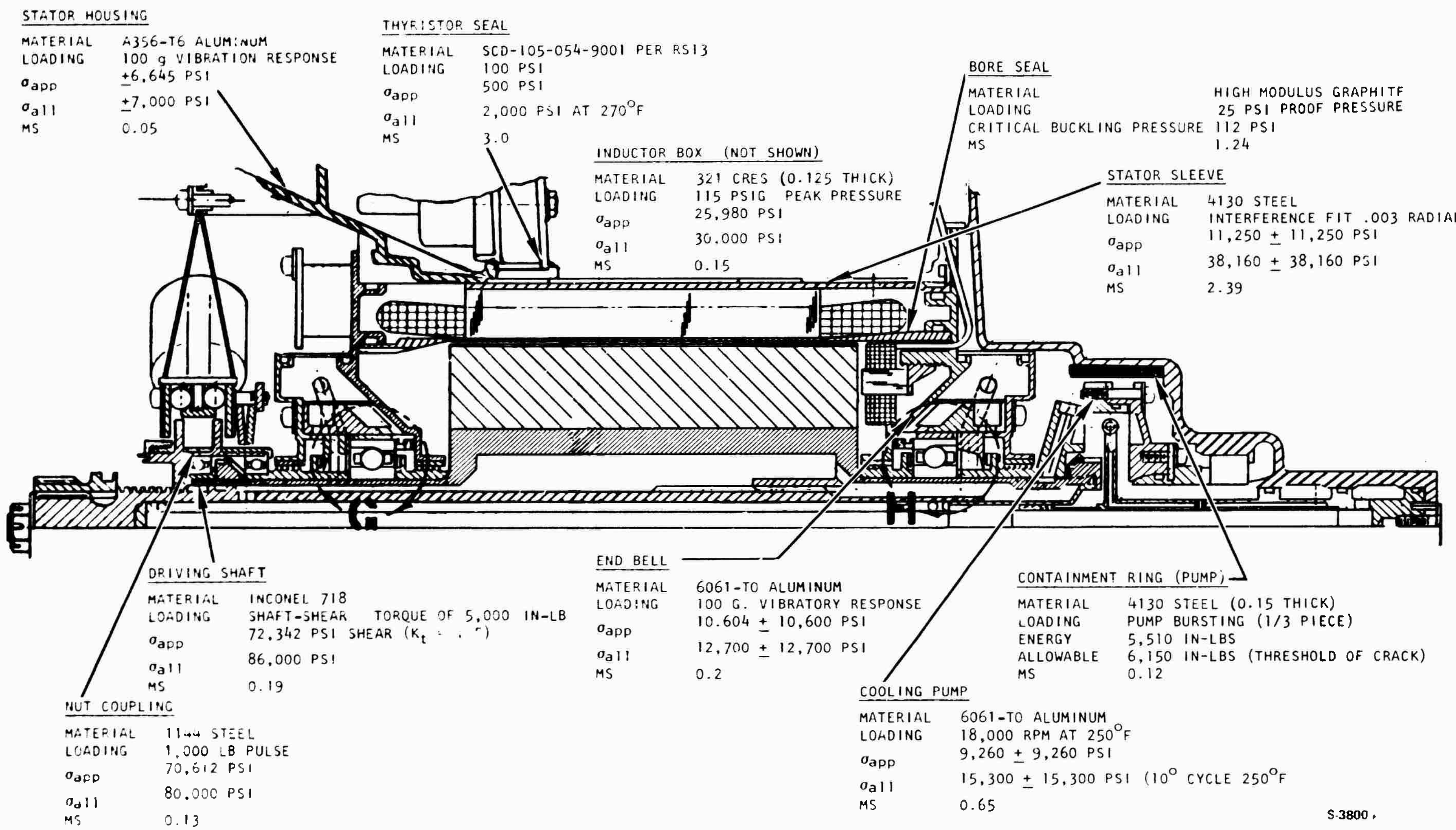


Figure 4-1. Generator Cross-Section Showing Materials, Loading, Applied Stresses (σ_{app}), Allowable Stresses (σ_{all}), and Margins of Safety

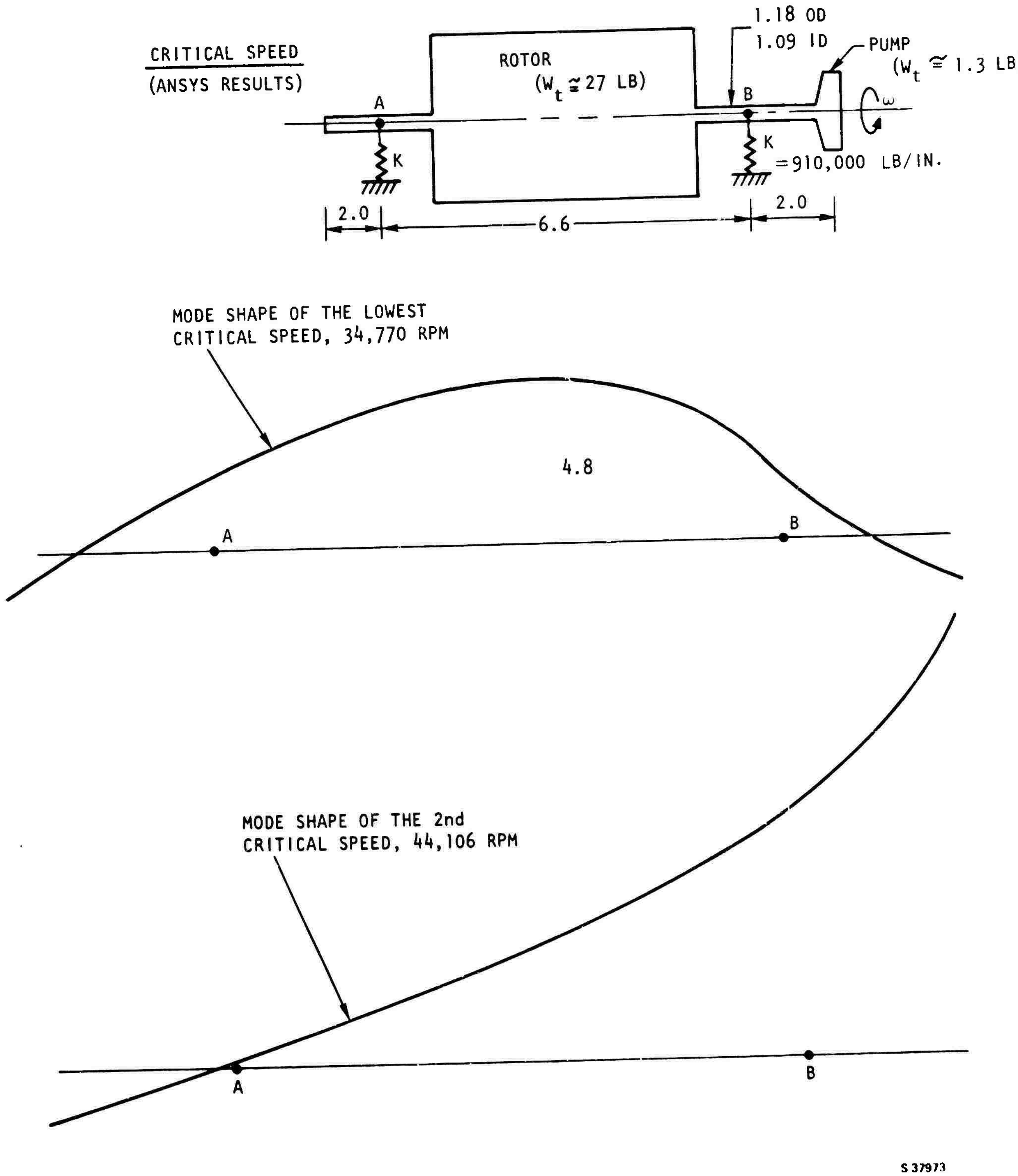


Figure 4-2. Rotor Assembly Critical Speed Calculation Results Summary

(Total Force Applied = 17 Pounds Laterally)

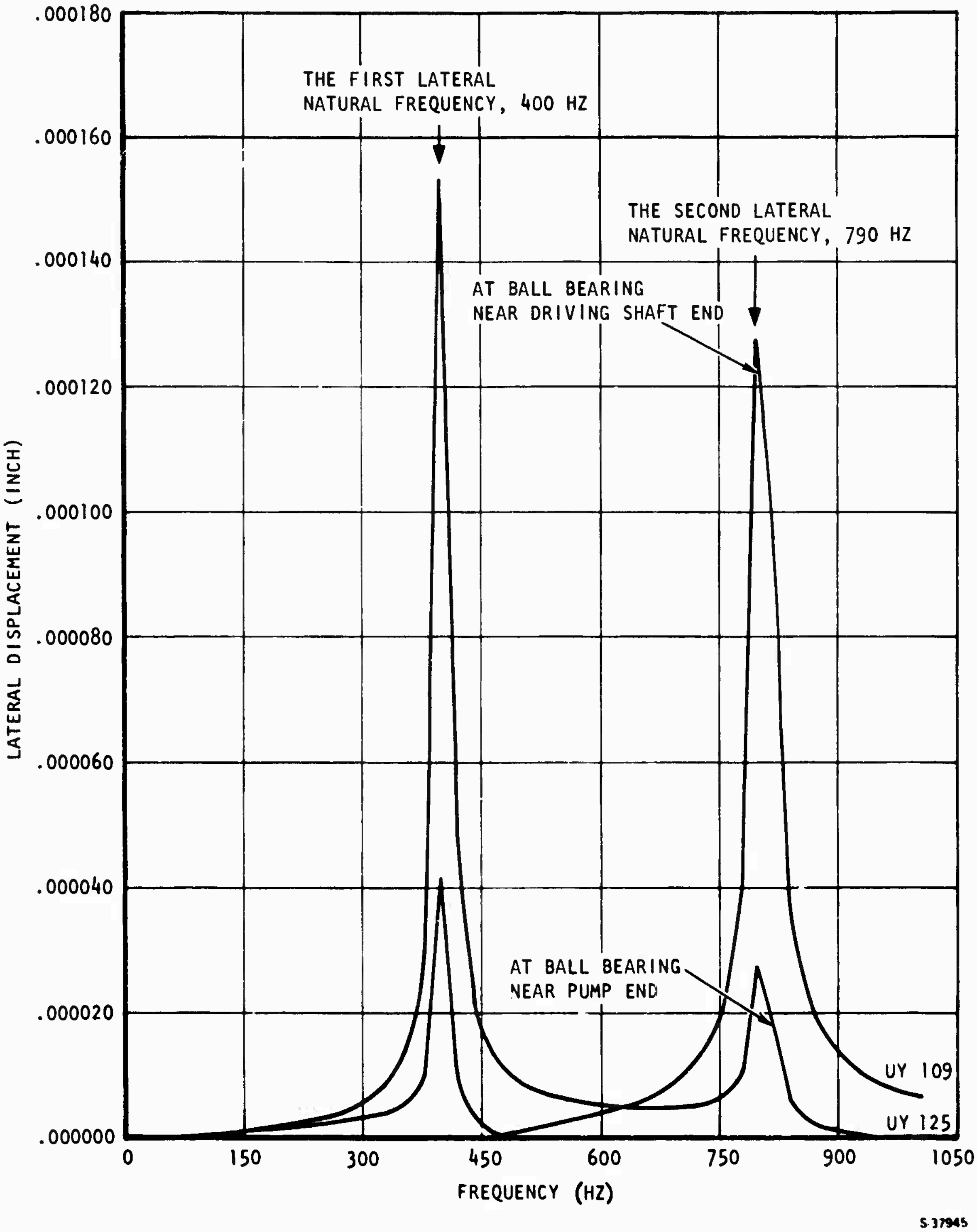


Figure 4-3. Lateral Harmonic Response of 270 VDC Permanent Magnet Generator Due to Force Excitation Applied at Rotor

GENERATOR THERMAL ANALYSIS

Thermal analysis, cooling loop design, and pressure drop calculations using Coolanol 25 fluid were performed on the generator assembly. The cooling circuit is shown on the outline drawing, 518988 (Figure 3-3), and properties of Coolanol 25 are shown in Figure 4-4. Pressure drop values for two flow rates are shown in Table 4-2.

TABLE 4-2. GENERATOR COOLING LOOP PRESSURE DROPS (COOLANOL 25 AT 250°F)

Location	Pressure Drop, psi Flow Rate		Remarks
	3.5 gpm	1.75 gpm	
SCR Heat Sinks (12)	52	14	Pin fin type heat sinks
Stator	13	6	Flow over end turns and the winding in slots and the OD shroud
Rotor	8	3	
Heat Exchanger	15	8*	From NADC, no filter
Lines to and from Heat Exchanger	5	2	10-foot by 5/8-inch and 10-foot by 1/2-inch tubes; 1.5 P to account for bends
Lines Between Components	7	3	24-inch by 3/8-inch, 5 sharp bends and 7 smooth bends
SCR Driver Cooling	3	1	
Ripple Inductor and Interphase Transformer	10	4	
Total	113	41	

*Estimated

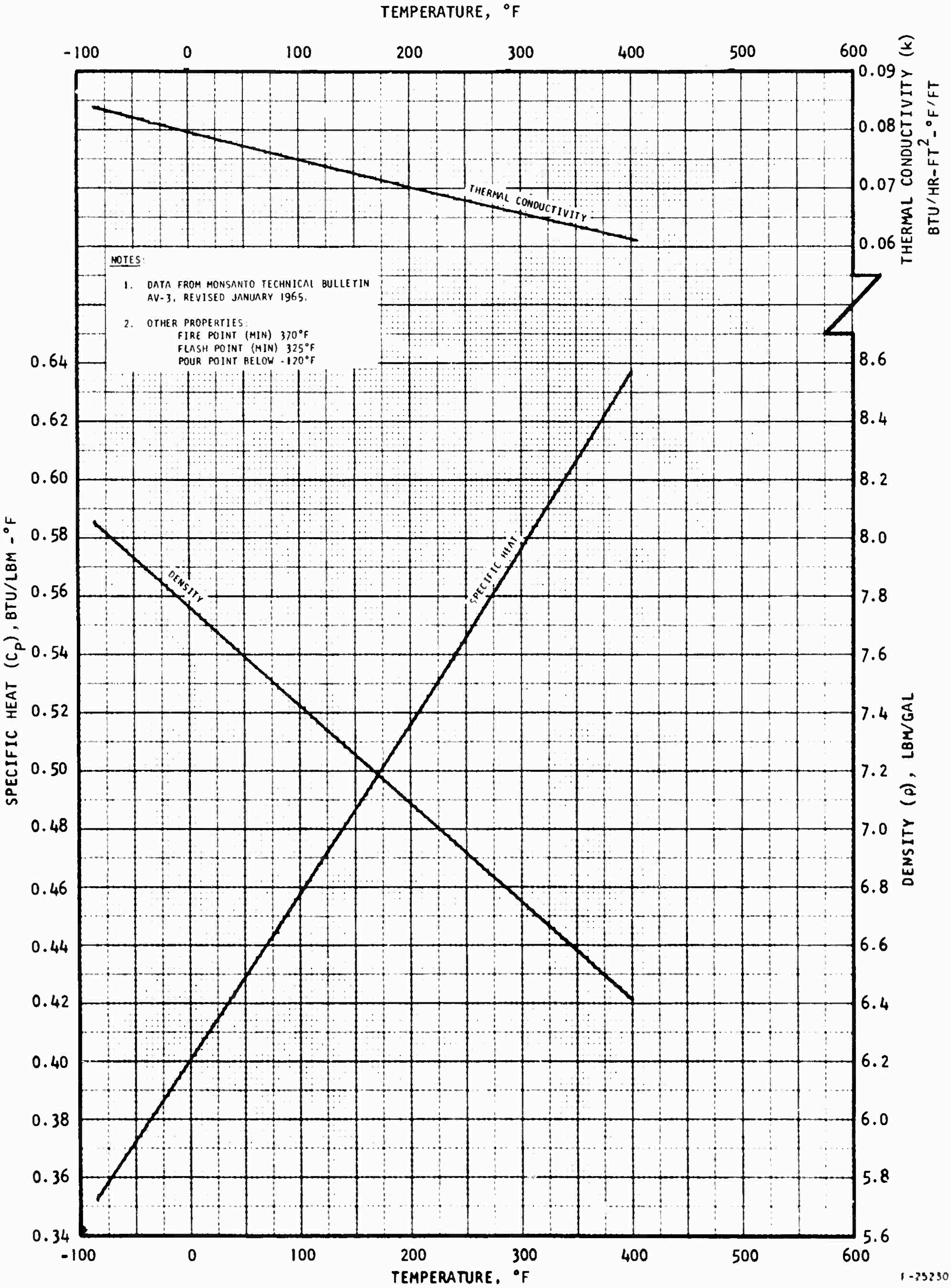


Figure 4-4. Typical Properties of Monsanto Coolanol 25 Fluid

Stator pressure drop predictions have been verified experimentally using a test stator housing assembly. The generator steady-state thermal analysis was performed based on the loss breakdown shown in Table 4-3. Temperatures were calculated at the thermal nodes shown in Figures 4-5 and 4-6. Results of the analysis are presented in Tables 4-4, 4-5, and 4-6.

POWER ELECTRONICS

The Power Electronics consist of the following components and subassemblies:

- Thyristor (546306)
- Interphase Transformer (2047031)
- Ripple Filter Capacitor (546309)
- Ripple Inductor (546310)
- Thyristor Driver Transformer (546311)
- SCR Driver (546315-1)

The circuit geometry is of two three-phase, full-wave rectifiers operated in parallel, phase displaced by 30 electrical degrees. An interphase transformer (ITP) is used to combine the two resulting six-pulse PDR outputs, producing a 12-pulse-per-cycle dc voltage. An L-C filter circuit at the output reduces the ripple voltage (see Figure 3-14).

The SCR driver circuit is typical of that shown in Figure 4-7. The drive circuit output waveform is a nonsymmetrical rectangular wave which is of positive polarity for 120 degrees, corresponding to the thyristor "on" interval, and is of negative polarity for 240 degrees, corresponding to the thyristor "off" interval. This design approach provides maximum gate circuit efficiency since it terminates drive at the end of thyristor conduction, eliminating the otherwise forward-biased junction (gate, cathode) during the 60 degrees of forward voltage remaining. During the 240-degree thyristor "off" interval the gate/cathode junction of the thyristor is reverse biased. The forward voltage-blocking capability of the thyristor is enhanced by reverse biasing of its gate/cathode junction, since in this state the gate is desensitized.

The thyristor driver transformer takes advantage of the constant volt/second relationship of the generator auxiliary power source. Over the regulation speed range, the voltage from the auxiliary power winding increases; i.e., as the frequency increases so does voltage. The resultant constant volt/second characteristic made possible a lightweight (optimum) driver transformer design. Special Supermendor tape-wound cores were designed and purchased for the thyristor drives.

TABLE 4-3. ELECTRICAL LOSSES, KW (400°F STATOR TEMPERATURE)

	9,000 rpm			18,000 rpm	
PU load	1.25	0	1.0	1.25	1.0
Stator copper	2.85	0	1.82	2.85	1.82
Stray	0.095	0	0.060	0.190	0.121
Pole head	0.076	0.033	0.060	0.220	0.176
Teeth	0.397	0.470	0.420	0.932	0.985
Core	0.435	0.515	0.460	1.017	1.075
TOTAL:	3.85	1.02	2.82	5.21	4.18

TABLE 4-4. GENERATOR THERMAL SUMMARY (MAXIMUM TEMPERATURES AND LOSSES)

Steady-State at 1.0 PU, 18,000 rpm, 3.5 gpm, Coolanol 25		
Location	Maximum Temp, °F (°C)	Loss at 400°F, Watts
Stator Conductor	335 (168) at Node 14	1941
Stator Back Iron	348 (175) at Node 18	1075
Stator Teeth	351 (177) at Node 16	985
Rotor	342 (172) at Node 5	176
Bearings	311 (155) at Node 28	60
Coolanol 25 Inlet	250 (121) at Node 50	—
Coolanol 25 Outlet	268 (131) at Node 57	—

TABLE 4-5. GENERATOR THERMAL SUMMARY
(SCR JUNCTION AND HEAT SINK TEMPERATURES)

Steady-State Condition		
	• Loss 38 watts/SCR, total 12 SCRs • Coolanol 25 at 250°F	
Flow	SCR Junction Temp °F (°C)	Heat Sink Temp °F (°C)
1.75 gpm	289.49 (143.04)	265.50 (129.71)
3.5 gpm	284.49 (140.26)	260.50 (126.93)

TABLE 4-6. AUXILIARY STATOR THERMAL SUMMARY

At 18,000 rpm and 250°F, Coolanol 25	
• Copper Winding Loss = 24 watts at 350°F • Teeth Loss = 57 watts • Core Loss = 43 watts • The stator is cooled by conduction with a minimum of 2-in^2 conduction path between stator core and aluminum end bell	
Location	Maximum Temp, °F (°C)
Copper Winding	383 (195)
Teeth	386 (197)
Core	383 (195)

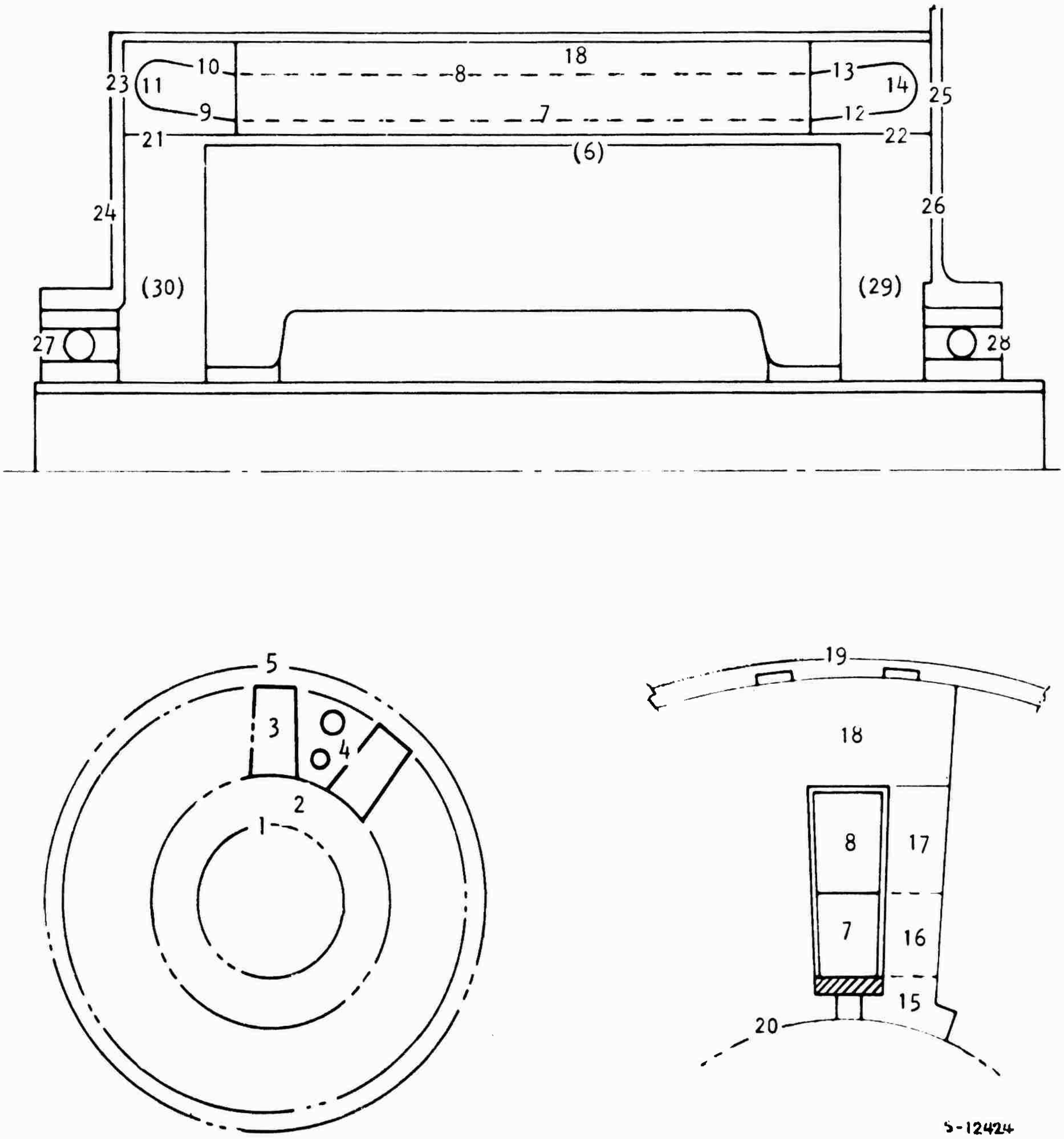


Figure 4-5. Generator Thermal Nodal System

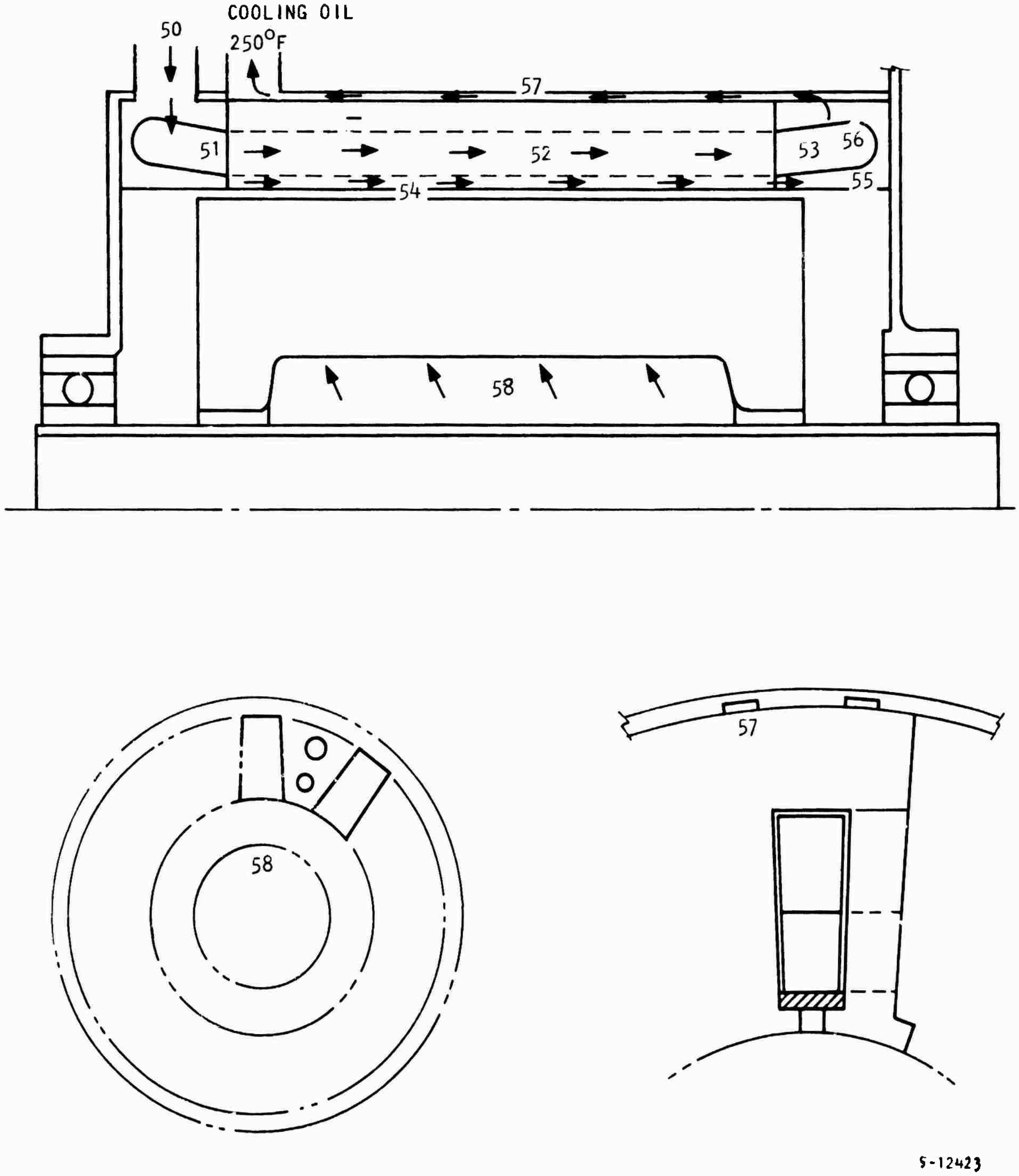


Figure 4-6. Generator Oil Stream Nodes

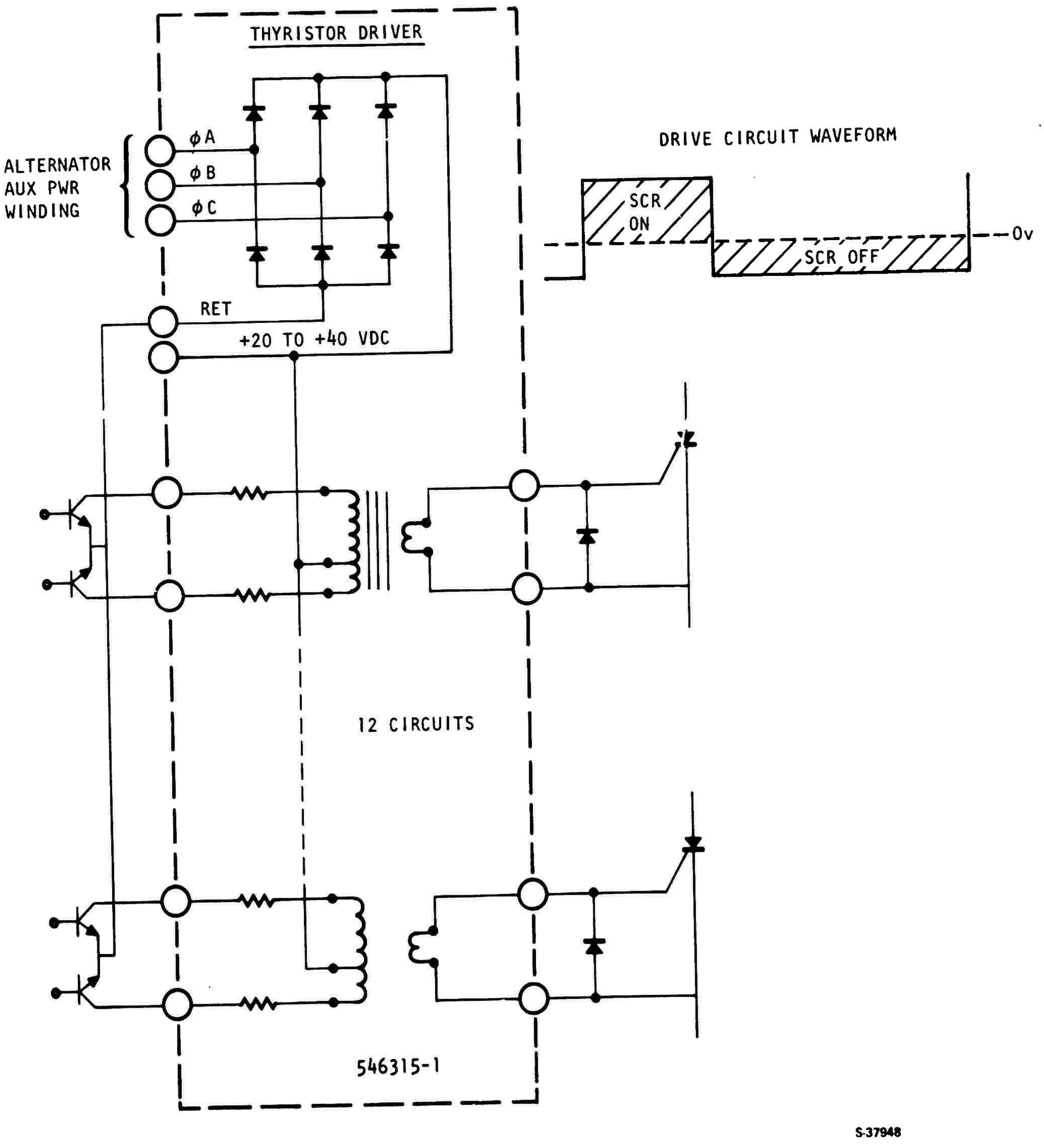


Figure 4-7. Typical SCR Drive Circuit

COMPONENT DESCRIPTIONS

Thyristor (546306)

The device selected for this application is the 81 RLA silicon-controlled rectifier (SCR) from International Rectifier. High-temperature, high-speed devices of similar characteristics are available from Westinghouse, Type T-507.

Special grading of processed wafers for temperature, speed, and reverse blocking characteristics produced the house device 81 RLB120 thyristor. Special packaging, which removes the stud and machines the hexagonal flats from the base, results in the 546306 SCR.

Before the thyristor is complete as a subassembly, a pin fin heat exchanger is soldered to the machined copper base, as shown on drawing 2046645 (Figure 4-8).

Interphase Transformer (IPT) (2047031)

The IPT is constructed on a special core of 0.002-inch 3-percent silicon steel. The core was specified after affirming analysis empirically. An error in the original design resulted in core saturation. Re-analysis confirmed by test measurements resulted in the present design. The core is wound with aluminum strip over a "C" core configured for maximum core/conductor utilization. The final transformer, prior to installation in its oil containment enclosure, weighs 0.75 pound.

The finished IPT is liquid cooled and contained in a stainless steel pressure vessel as shown on drawing 2047027 (Figure 4-9).

Ripple Filter Capacitor (546309)

The ripple filter capacitor is aluminum foil over polysulfone dielectric film, oil impregnated. The foil is wound in two coils and then fitted into the special can shown in Figure 4-10. The envelope of the ripple filter capacitor was necessitated by the space available within the alternator envelope.

The resulting capacitor cools via conduction through its mounting hardware, is capable of operating at temperatures above 150°C, will withstand 100 g vibration, will operate at altitudes beyond 65,000 feet, and is small and relatively reliable, being of extended foil construction using welded heavy braid for its termination.

Ripple Inductor (546310)

The ripple inductor is wound on a 3.5-percent grain-oriented silicon steel "C" core, using polyimide-coated high-temperature copper magnet wire. The finished inductor is braced for shock and vibration and double-impregnated with polyimide varnish. The finished inductor is assembled in a stainless steel pressure vessel, as shown on drawing 2046650 (Figure 4-11), and liquid cooled when connected to the system.

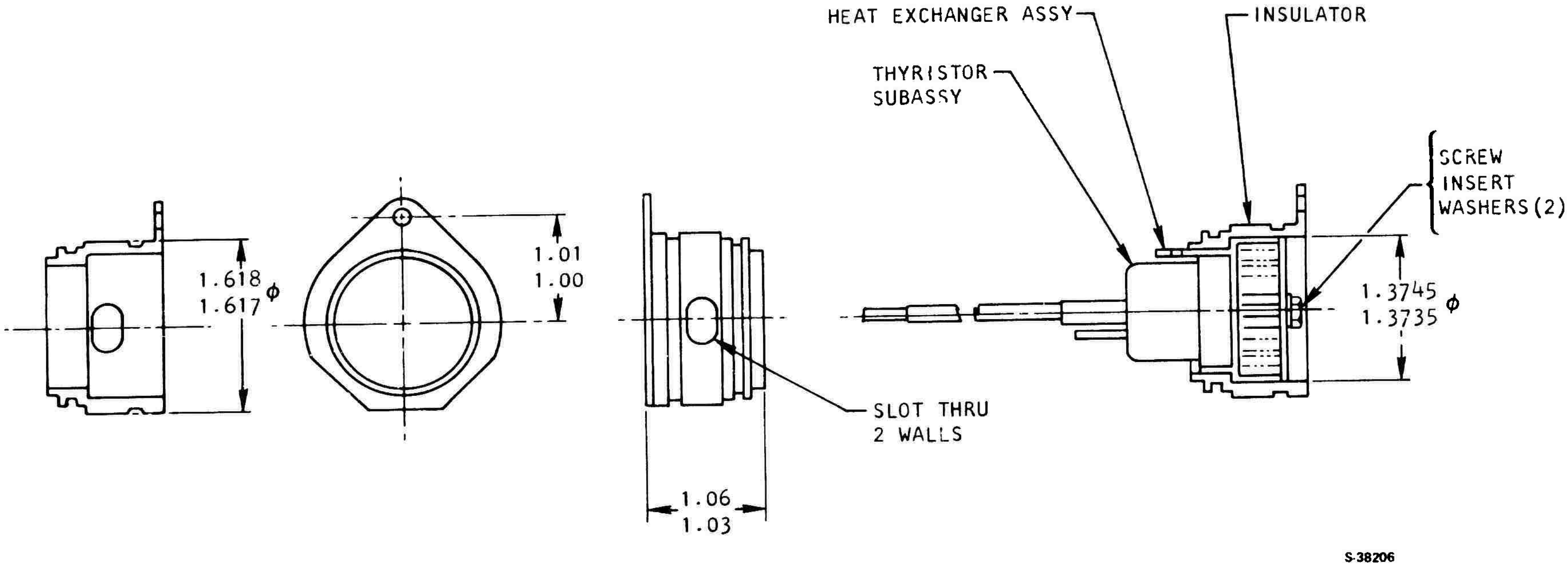


Figure 4-8. Thyristor Assembly, 2046645

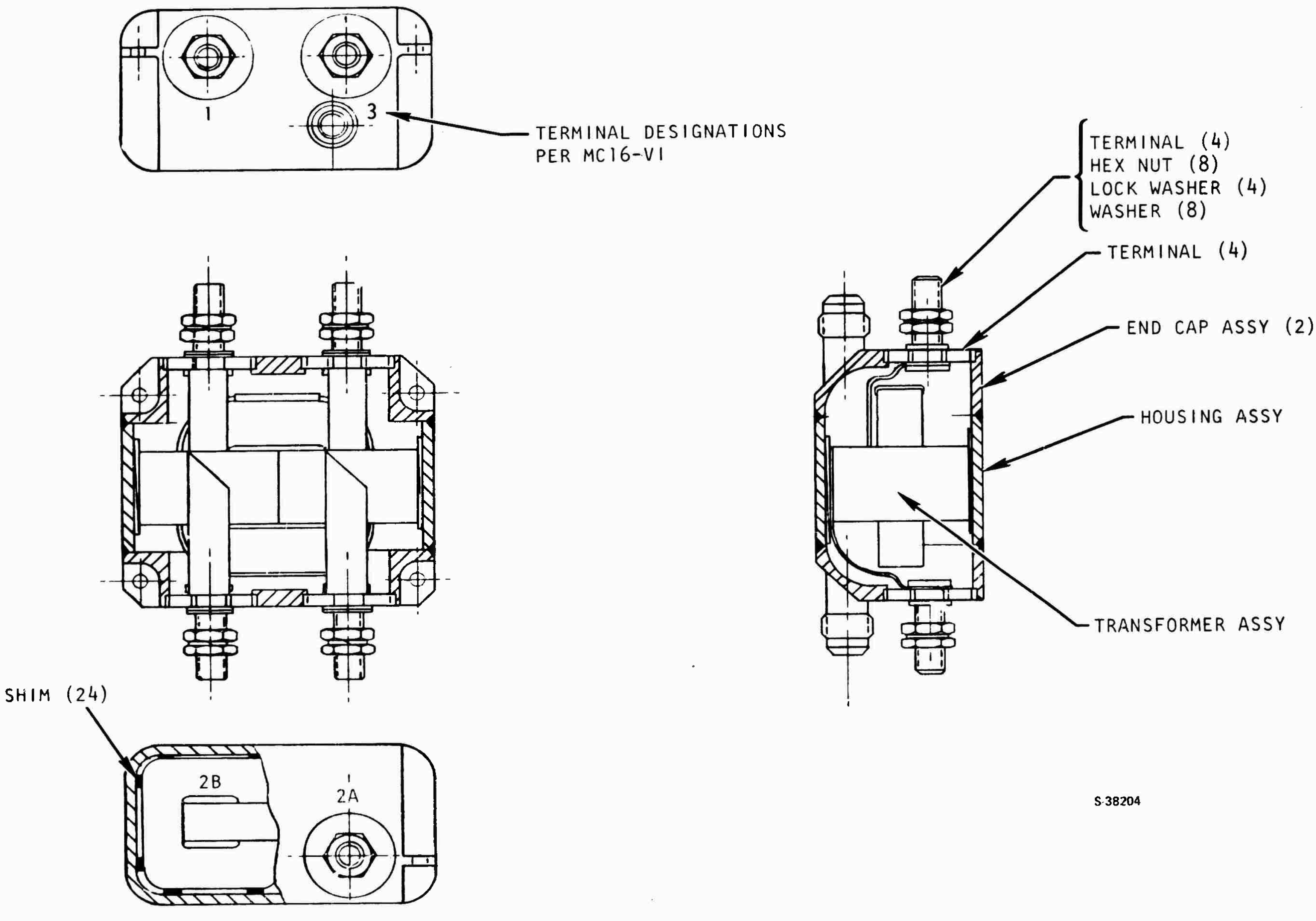


Figure 4-9. Interphase Transformer Assembly, 2047027

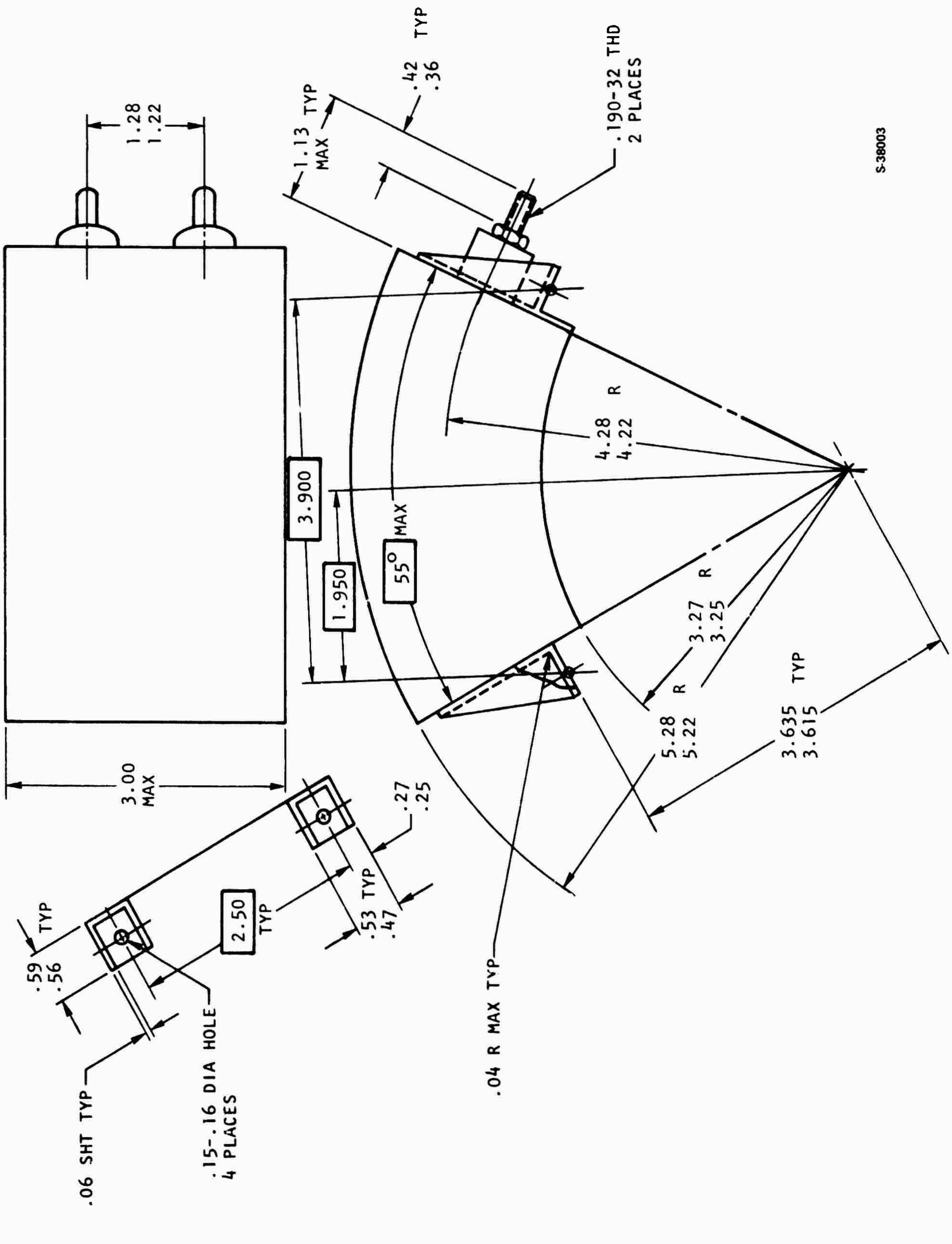


Figure 4-10. Ripple Filter Capacitor, 546309

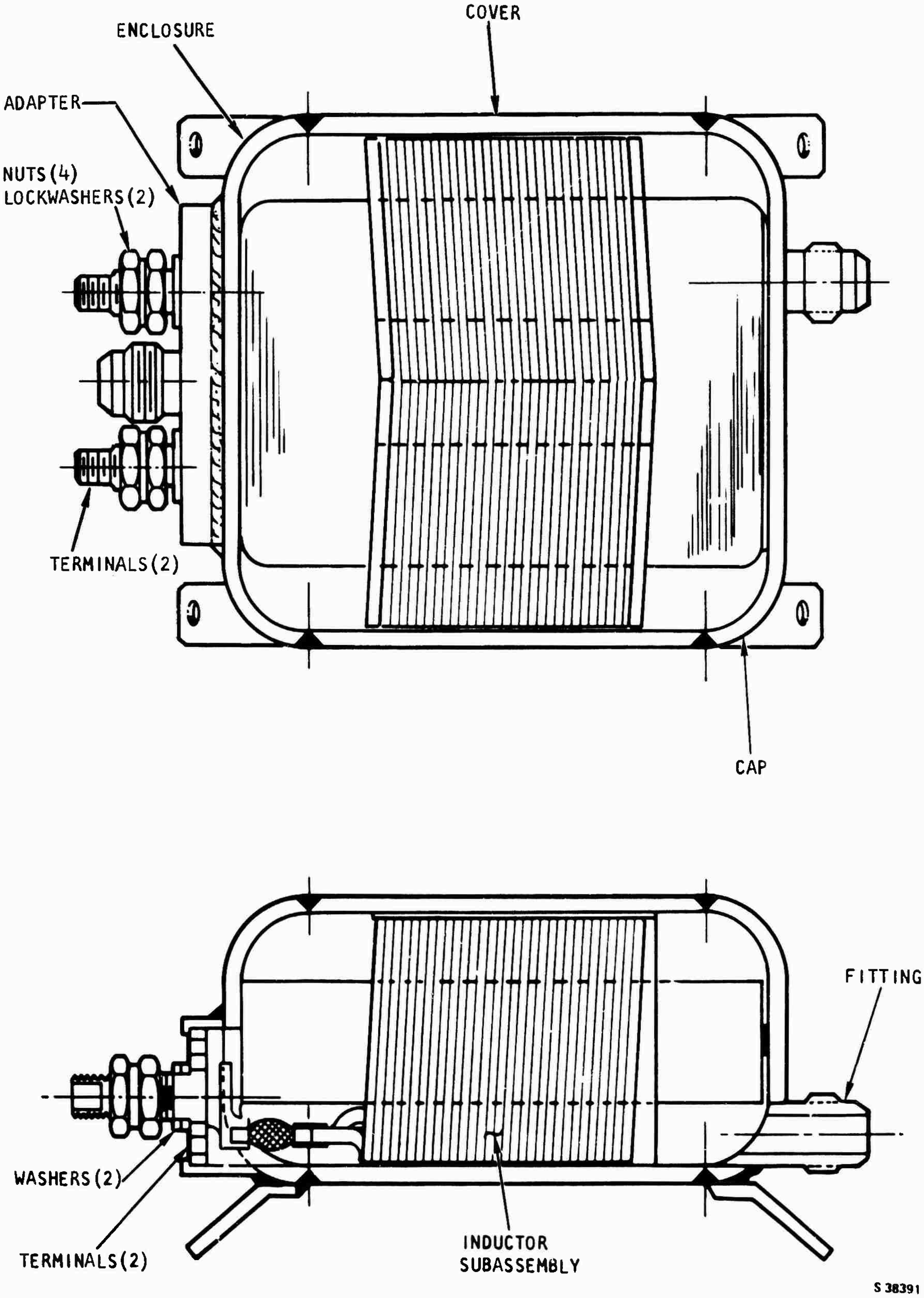


Figure 4-11. Ripple Inductor Assembly, 2046650

Thyristor Driver Transformer (546311)

The thyristor driver transformer is fabricated using a special Supermendor, toroidal tape-wound core and high-temperature insulated copper magnet wire. A very small, lightweight device results. The transformer was designed to be convection cooled with a reductor in close proximity to an oil-cooled surface within the generator package. Twelve such transformers are arranged on a toroidal PC board to control the PDR thyristors.

GENERATOR CONTROL UNIT

Detailed descriptions of the analytical design work involving the major subassemblies and components of the generator control unit are presented in the following paragraphs.

THERMAL ANALYSIS

A preliminary thermal analysis was conducted on the 270 vdc GCU to determine the steady-state temperature of certain high-wattage solid-state devices and the following printed circuit boards with integral aluminum heat sinks:

- A1 power supply board
- A2 power supply board
- Microprocessor board
- Input/output (I/O) board
- PDR timing board (2 each per GCU)

The ambient corresponds to the operating condition (85°C and 7.5 psia) at point A on Figure 4-12, which shows the compartment ambient temperature variation with altitude for unconditioned compartments of high-performance aircraft. In the absence of installation data, it was assumed that the control box is unsupported. Therefore, the box is externally cooled by combined natural convection and radiation only.

Because of heat dissipation (59 watts total) and the high (85°C) ambient, it was estimated that the GCU components would be subjected to relatively high temperatures. In attempts to reduce the temperature of the components, six thermal models were analyzed. As a guideline a maximum temperature of 110°C is used for the printed circuit board. 150°C maximum is used for the diodes and 125°C maximum is used for the integrated circuits and transistors.

Thermal Model

Figure 4-13 shows the basic thermal model (model 1) of the GCU and Table 4-7 gives a description of each node. Model 1 employs one finned heat sink on top of the box and three aluminum spacers between the A1 board heat sink (No. 23) and A2 board heat sink (No. 26). Each spacer has an annular conduction area with an inner diameter of 1/8 inch and an outer diameter of 3/8 inch. The thickness of each wall in the box is listed in Table 4-7.

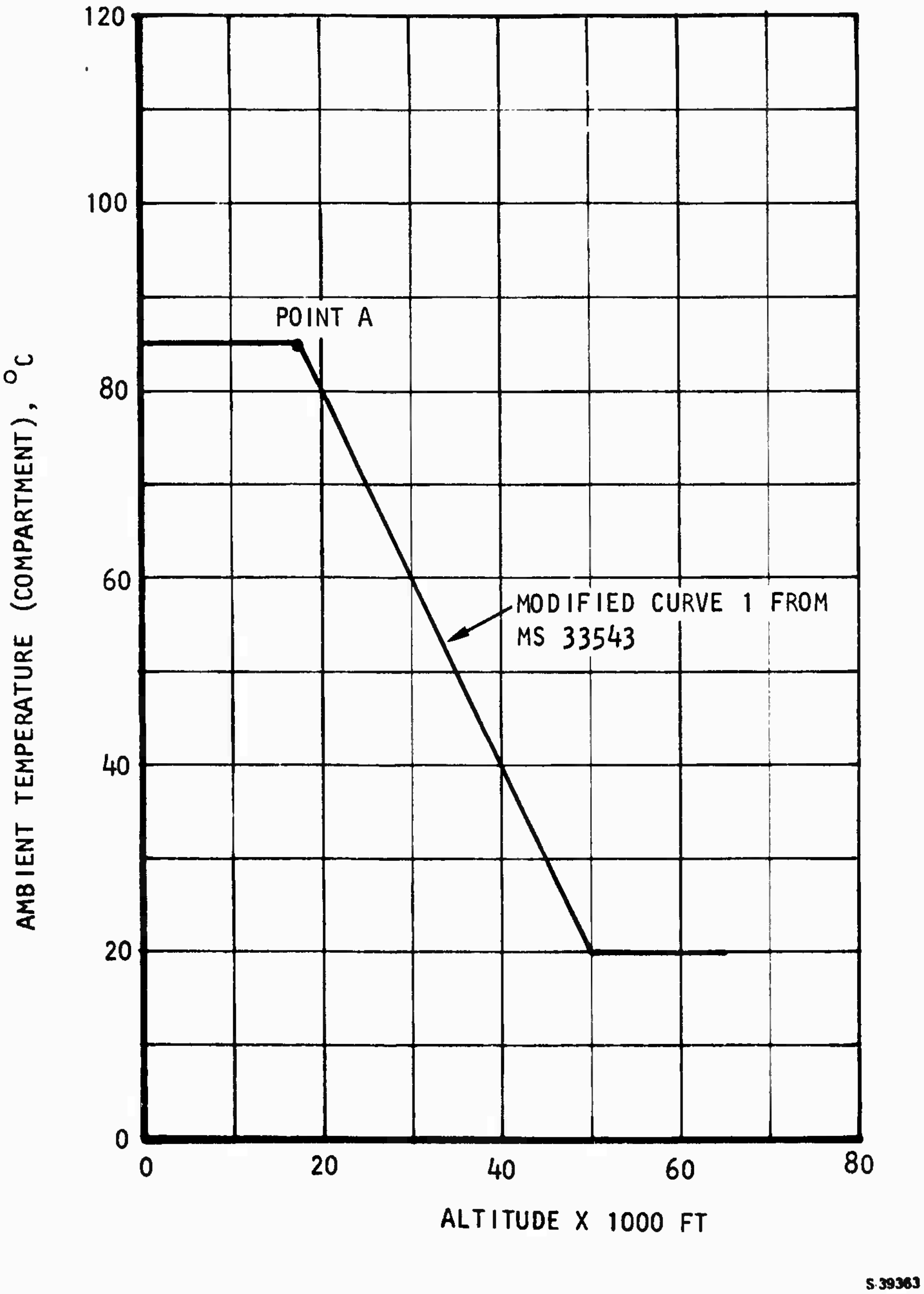
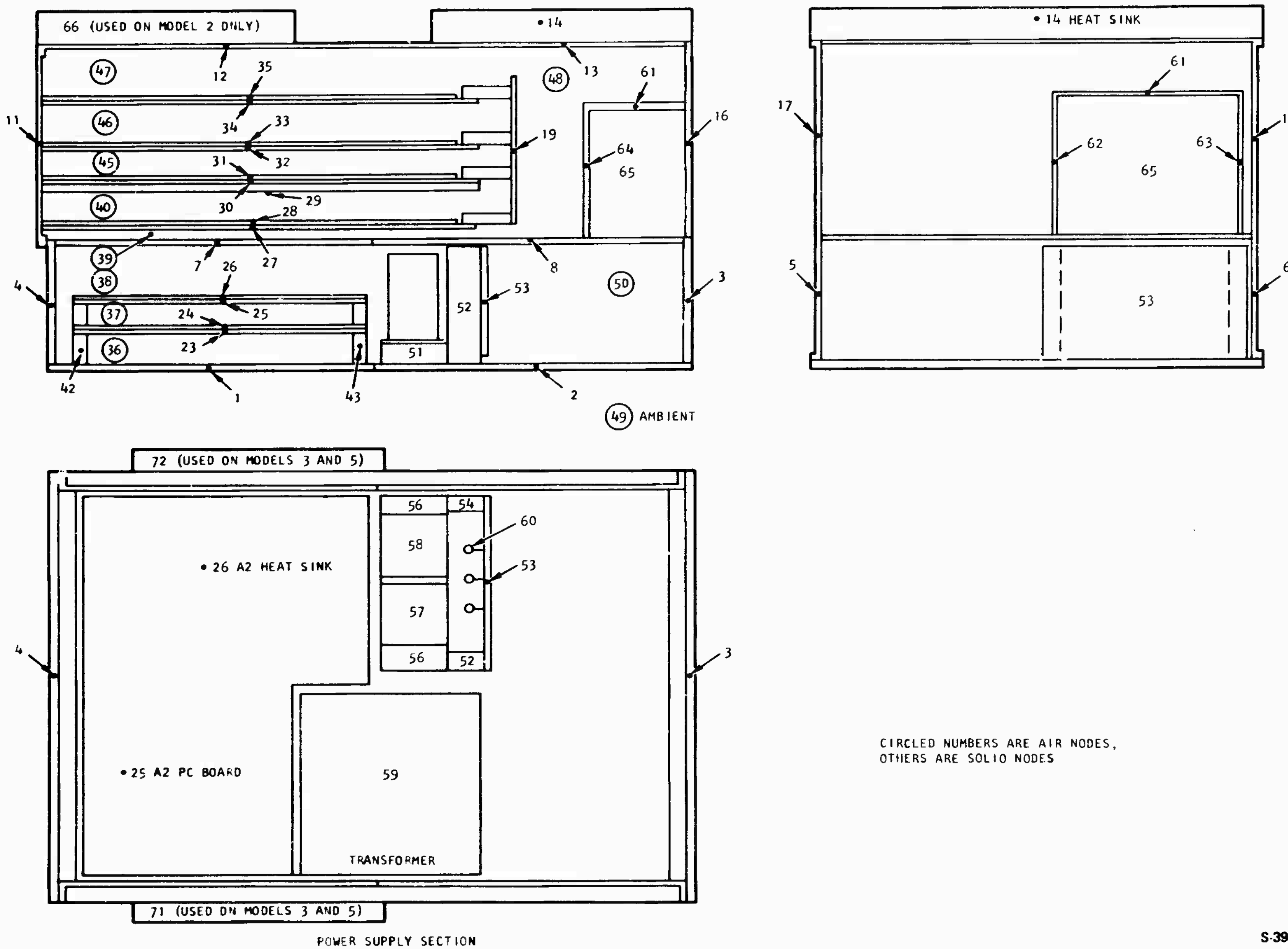


Figure 4-12. Ambient Environment for Thermal Analysis



S-39364

Figure 4-13. Thermal Model of 270-Volt GCU (Model 1)

TABLE 4-7. NODE DESCRIPTION

Node	Description
1,2	Aluminum bottom plates, 0.188 in. thick
3,16	Rear wall, aluminum, 3 = 0.08 in. thick; 16 = 0.063 in. thick
4,11	Front wall, aluminum, 4 = 0.08 in. thick; 11 = 0.050 in. thick
5,6,17,18	Side wall, aluminum, 0.070 in. thick
7,8	Power supply top wall, 0.070 in. thick (Models 1, 2, 4) 0.10 in. thick (Models 3, 5, 6)
9,10	Rubber pad
12,13	Top cover plate, aluminum, 0.05 in. thick
14	Top finned heat sink, Thermalloy 6180 extrusion, aluminum
15,22	Spare
19	Connector support board, printed circuit board material
20,21	Connector support board brackets
23	A1 board aluminum heat sink, 0.062 in. thick
24	A1 printed circuit board, 0.062 in. thick
25	A2 printed circuit board, 0.062 in. thick
26	A2 board aluminum heat sink, 0.062 in. thick
27	Microprocessor printed circuit board, 0.062 in. thick
28	Microprocessor aluminum heat sink
29	Microprocessor top shield plate, 0.04 in. thick
30	I/O printed circuit board, 0.062 in. thick
31	I/O board aluminum heat sink, 0.062 in. thick
32,34	PDR printed circuit board, 0.062 in. thick
33,35	PDR board heat sink, 0.062 in. thick
36,37,38,50	Air nodes in power supply section
39,40,45 to 48	Air nodes in top section of unit
49	Ambient, 85°C and 7.5 psia (17,500 ft altitude)
51,52,54,55	L-shape bracket for power supply diode plate, aluminum
53	Power supply diode heat sink plate, aluminum, 0.1 in. thick

TABLE 4-7 (Continued)

Node	Description
56	Inductor platform, aluminum, 0.04 in. thick
57,58	Inductor
59	Transformer
60	Power supply diodes (8 diodes)
61 to 64	Internal walls, 0.065 in. thick
65,70	Air node, 70 is used in models 3 and 5 only.
66	Second top finned heat sink (used in Model 2 only)
42 to 44,67 to 69	Rectangular bar standoff for A1 board (42 to 44) and A2 board (67 to 69 for Models 3 and 5)
71,72	Side finned heat sink for Models 4 and 5

TABLE 4-8. POWER DISSIPATION SUMMARY

Component	Power Dissipation, watts		Total Power on Board or Chassis, watts
	To Aluminum Heat Sink or Chassis	To Nonmetallic Board	
Power Supply Section			
A1 board	14.0	0.3	14.3
A2 board	5.1	0.7	5.8
Diode plate	11.9	---	11.9
Chassis-mounted parts	7.0	---	7.0
Microprocessor Board	3.9	0.11	4.01
I/O Board	0.96	0.3	1.26
PDR Timing Board 1	1.8	0.54	2.34
PDR Timing Board 2	1.8	0.54	2.34
Top Finned Heat Sink	10.0	---	10.0

The other thermal models are listed below.

Model 2--This is the same as model 1 with a second heat sink (No. 55) on top of the box.

Model 3--This model uses one top finned heat sink and the A2 board heat sink is connected to three aluminum rectangular standoffs (Nos. 67, 68, 69) which are connected to the power supply top plate (No. 7). The standoffs between the A1 printed board (No. 24) and A2 printed board (No. 25) were deleted.

Model 4--This is the same as model 1 with a vertical fin heat sink (No. 71 or 72) mounted on each side wall.

Model 5--This is the same as model 3 with a vertical fin heat sink (No. 71 or 72) mounted on each side wall.

Model 6--This is the same as model 3 except that aluminum cylindrical standoffs are used in place of the rectangular standoffs because of space limitation.

Discussion and Results

The internal power dissipation breakdown for the 270-volt GCU is given in Table 4-8. The total power dissipation is 59 watts and the free space power density is 0.11 watt/sq in. Of the total power, 66 percent or 39 watts is dissipated in the power supply section, which accounts for higher temperatures in this section as compared to the upper section where the PDR boards are located.

Note that at the time of the analysis some of the printed circuit boards and integral aluminum heat sink designs were not complete. Therefore, certain assumptions about the circuit board heat sinks were made in order to facilitate the analysis. Such assumptions included a 60-percent heat sink for the A1 board, a 40-percent heat sink for the A2 board, and a 20-percent heat sink for the microprocessor and I/O boards. The PDR board design was available and it was determined that each PDR board usea a 35-percent heat sink. With the assumed heat sinks the thermal results in Table 4-9 show that the temperatures for the microprocessor (Nos. 27 and 28), I/O (Nos. 30 and 31), and PDR (Nos. 33 to 36) boards are acceptable for all thermal models, since the temperatures are below the guideline value of 110°C. However, the A1 board (Nos. 23 and 24) and the A2 board (Nos. 25 and 26) is acceptable only for Models 3 and 5.

In addition to high or marginal temperatures predicted for the A1 and A2 boards, Table 4-9 also shows that the average temperature of the diode connected to diode plate No. 53 will be about 172°C. This is considerably above the desirable guideline level of 150°C.

Supplementing the results in Table 4-9, Figures 4-14 and 4-15 show the temperature at various locations in the control box for model 1 and model 6, respectively. The temperature maps for models 2 through 5 were omitted for brevity.

TABLE 4-9. TEMPERATURE SUMMARY OF 270-VOLT GCU

Node	Temperature, °C					
	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6
1	107	106	106	105	104	106
5	102	101	102	99	100	102
7	104	104	106	103	104	105
12	96	94	96	96	96	96
14	98	97	98	98	98	98
17	99	99	99	99	99	99
23	112	112	110	111	109	111
24	113	112	110	111	109	111
25	118	117	108	116	106	114
26	119	118	108	117	106	114
27	106	105	107	105	106	106
28	107	106	108	106	107	107
30	103	102	104	103	103	104
31	103	103	104	103	103	104
32	104	103	104	103	104	104
33	104	103	104	103	104	104
34	102	101	102	102	102	102
35	102	101	102	102	102	102
38	110	109	106	108	104	108
47	99	97	99	99	99	99
48	99	98	99	98	98	99
50	112	111	111	110	110	111
53	126	126	126	125	124	125
60	172	172	172	171	171	171
71	None	None	None	99	99	None
72	None	None	None	99	99	None

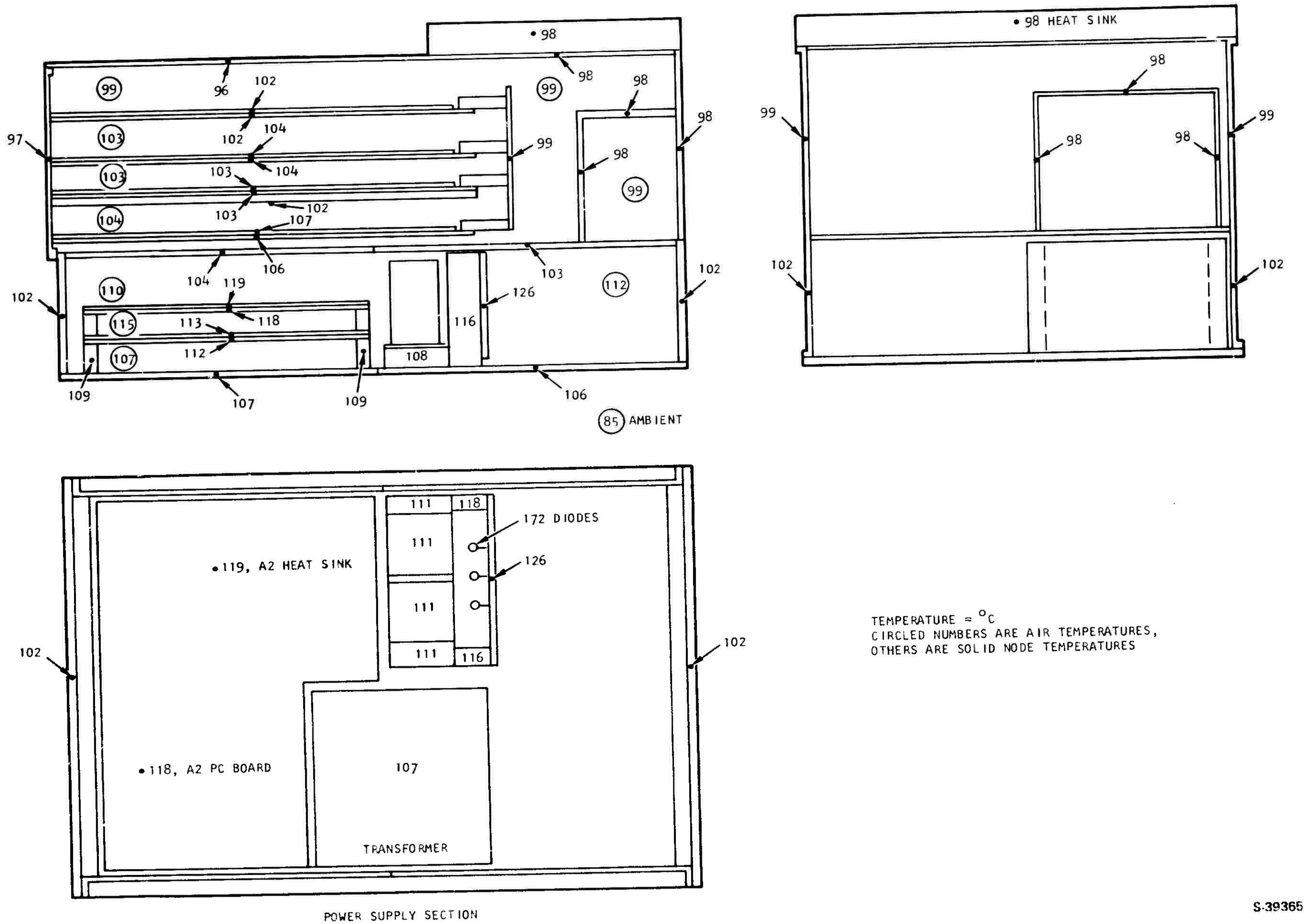


Figure 4-14. Model 1 Box Temperatures

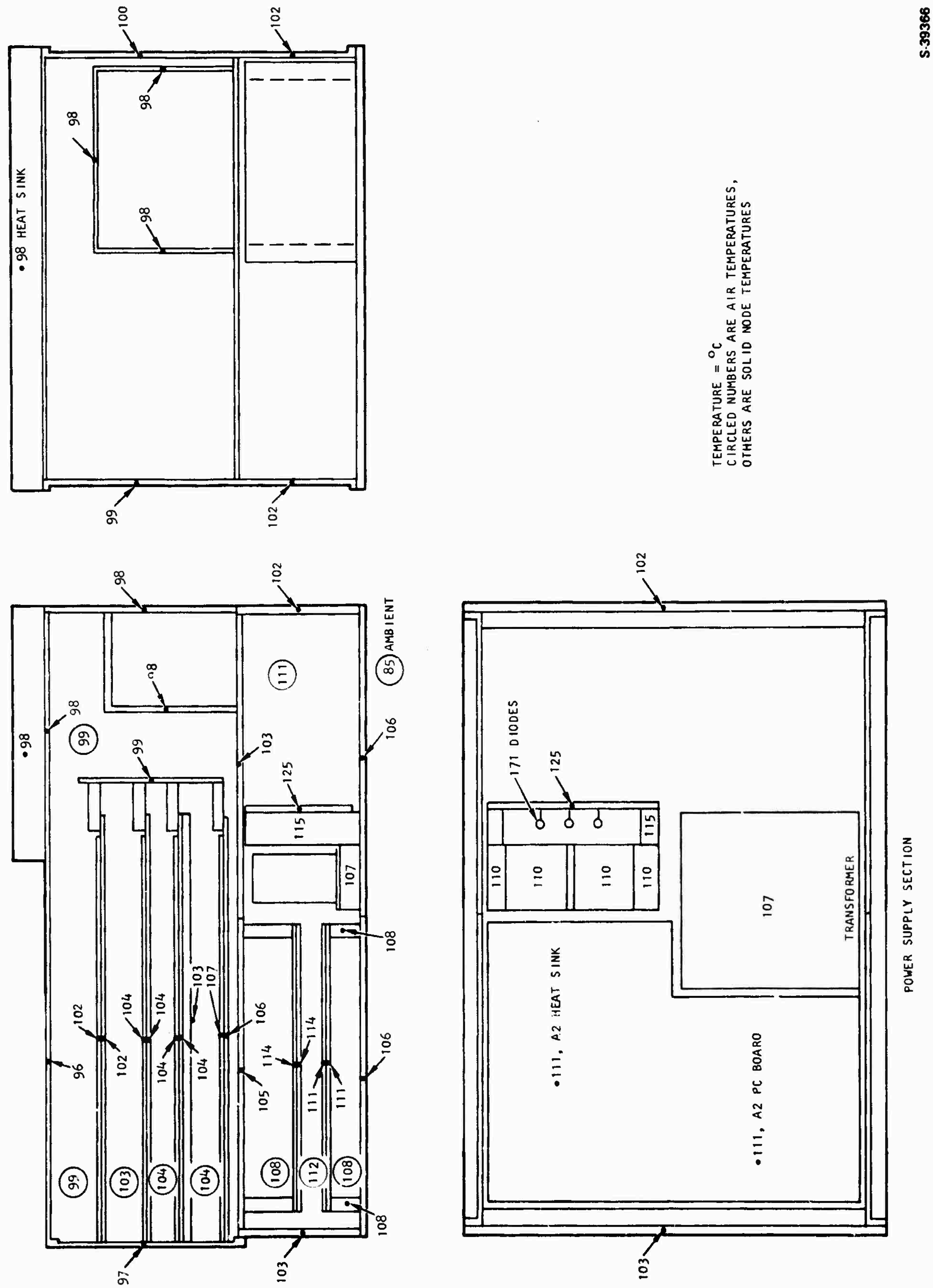


Figure 4-15. Model 6 Box Temperatures

Conclusion

Present indications are that only model 1 and model 6 are acceptable on the basis of design, weight, and time constraints but unacceptable on the basis of temperature requirements. Models 2, 4, and 5 do not offer sufficient temperature improvements to justify the increase in weight caused by the addition of extra finned heat sinks. With the exception of the diode in node 60, Model 3 is the preferred packaging method. Model 3 was used in packaging the GCU. The diode's maximum temperature of 172°C was considered acceptable for this phase of the effort, since its maximum rated temperature is 208°C.

CIRCUIT ANALYSIS

Microprocessor and Memory Board

Board A4 of the GCU contains the 8080 microprocessor and its associated circuitry. Drawing 2106389 (Figure 4-16) shows the schematic of the board and Figure 4-17 is the block diagram.

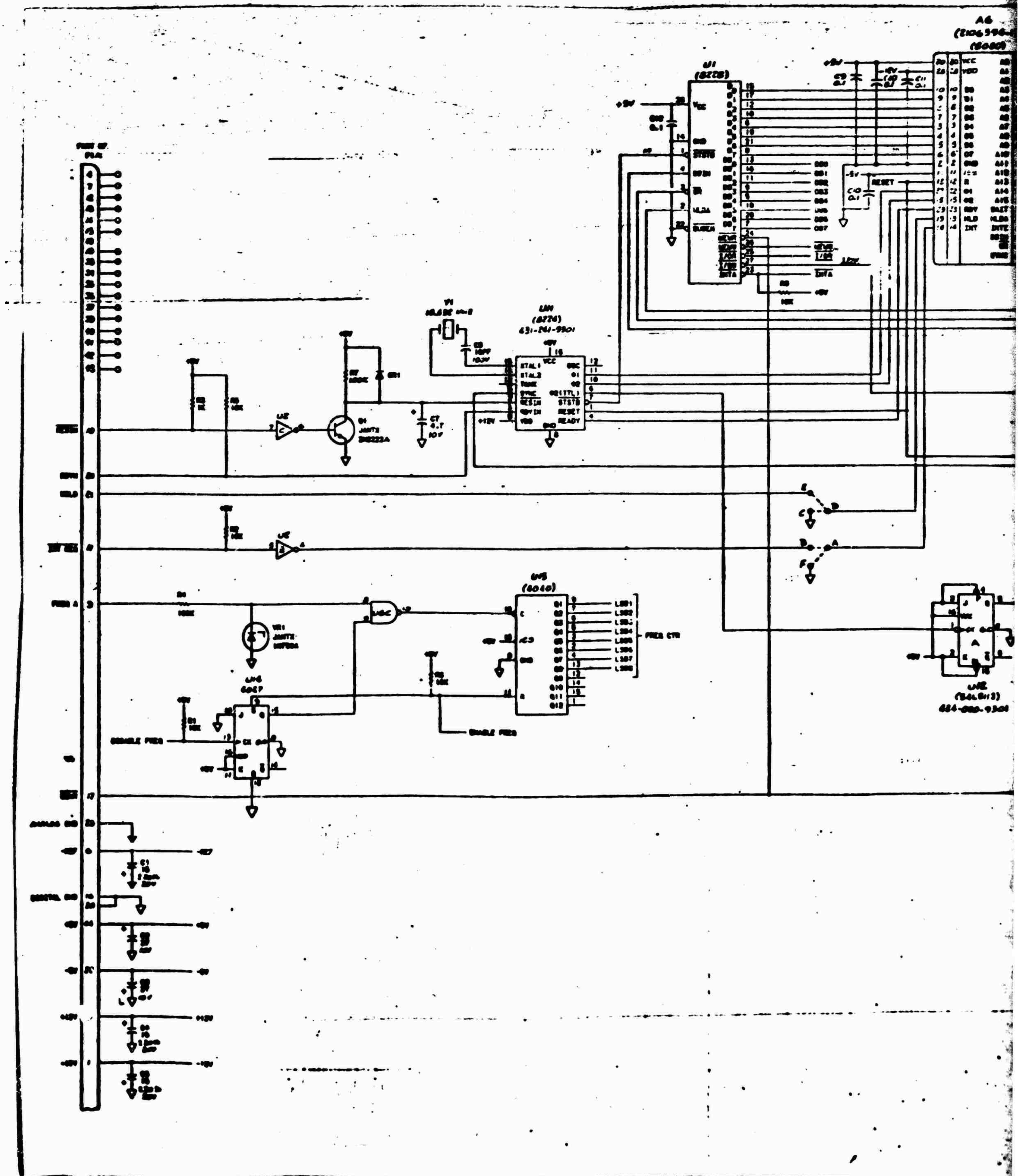
The address range for the EPROM is ØØØØ to hexadecimal Ø3FF. The 256 bytes of RAM are from address Ø400 to Ø4FF hexadecimal. The memory address decoding is very simple. When address bit 10 (AB10) is high, the RAM is selected, whereas if the same bit is low, the EPROM is selected.

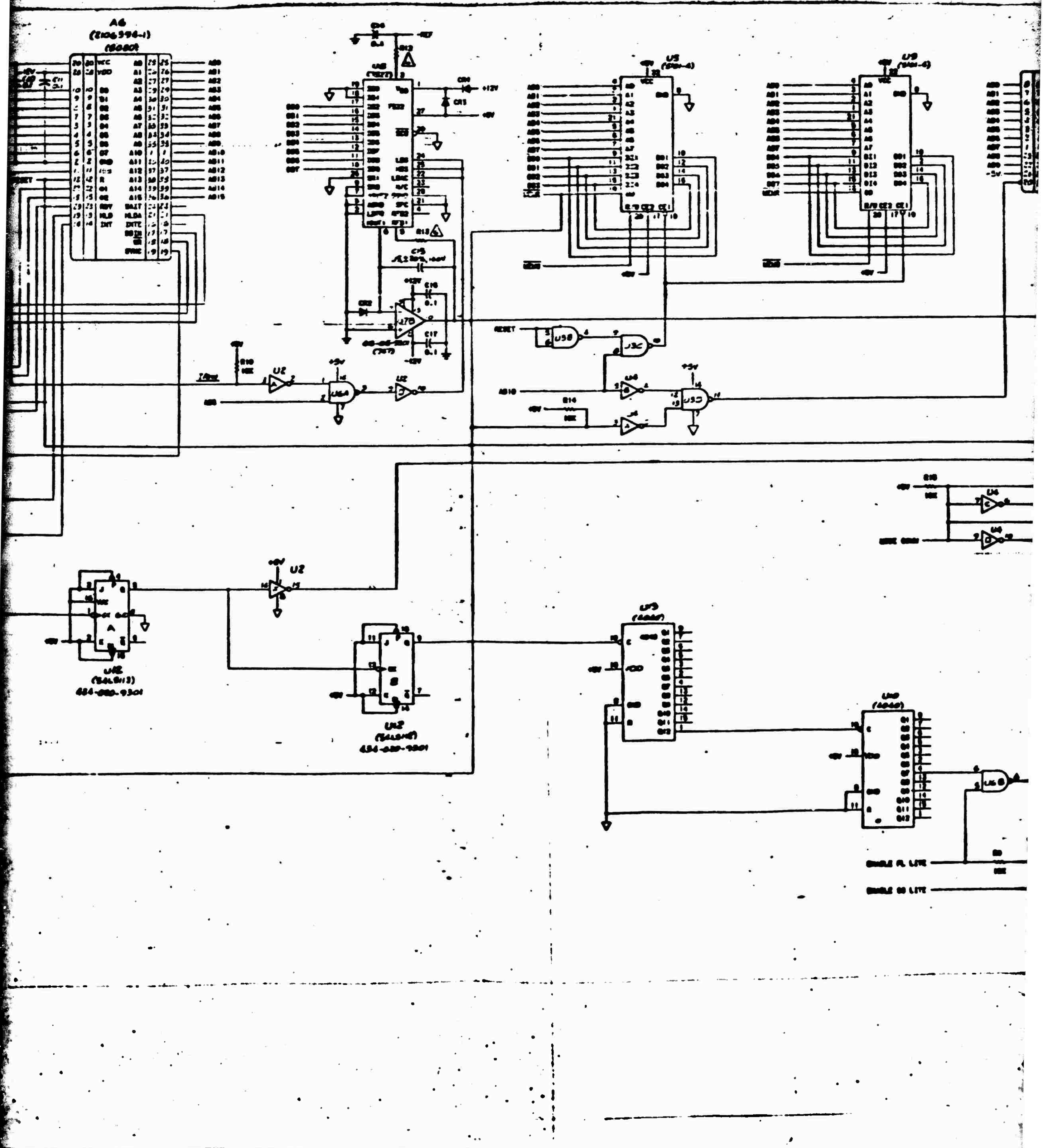
As far as I/O addressing is concerned, the 8080 can address nine different ports, four each for the two 8255 chips, and one for the D/A converter.

A5	A4	A3	A2	A1	A0	I/O Port
0	0	1	X	0	0	8255 #1 port A
0	0	1	X	0	1	8255 #1 port B
0	0	1	X	1	0	8255 #1 port C
0	0	1	X	1	1	8255 #1 control port
0	1	0	X	0	0	8255 #2 port A
0	1	0	X	0	1	8255 #2 port B
0	1	0	X	1	0	8255 #2 port C
0	1	0	X	1	1	8255 #2 control port
1	0	0	X	X	X	D/A converter

For a detailed description of the 8255 input and output ports, refer to "270V GCU Software".

FREQ A is an input which is brought to the A4 board from the PDR board A1. It is a sine wave whose frequency is directly proportional to the speed of the


A6
U1
(8228)
U14
(8224)
431-261-9301
U15
(4040)
U12
(54LS113)
484-080-9301
Y1
18.432 MHz
Q1
JANTX
2N2222A
FREQ CTR
ENABLE FREQ
DISABLE FREQ
ANALOG GND
DIGITAL GND
RESET
INTA



2

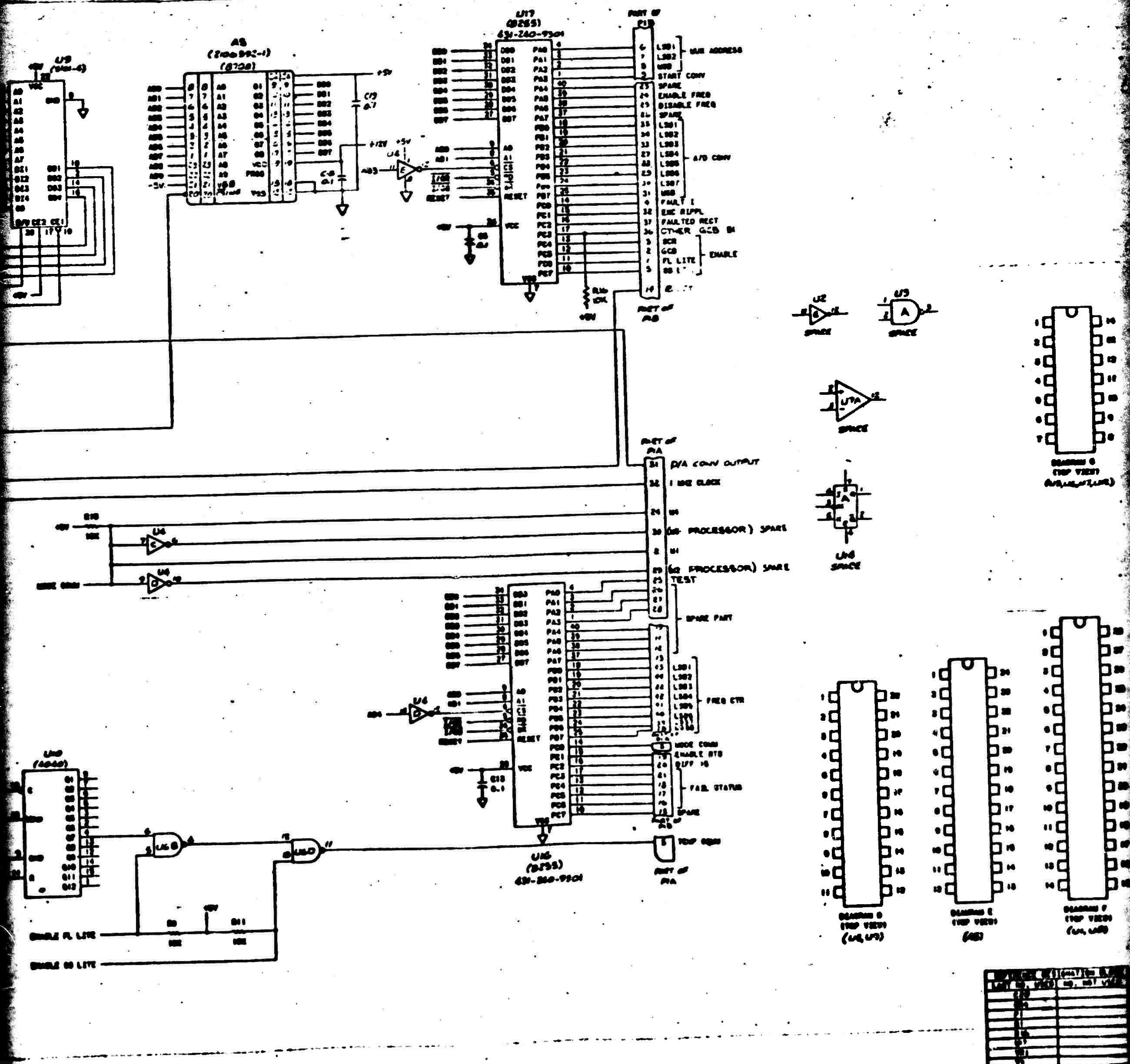


Figure 4-16

Schematic Wiring Diagram, Mi
and Memory Board, 2106389

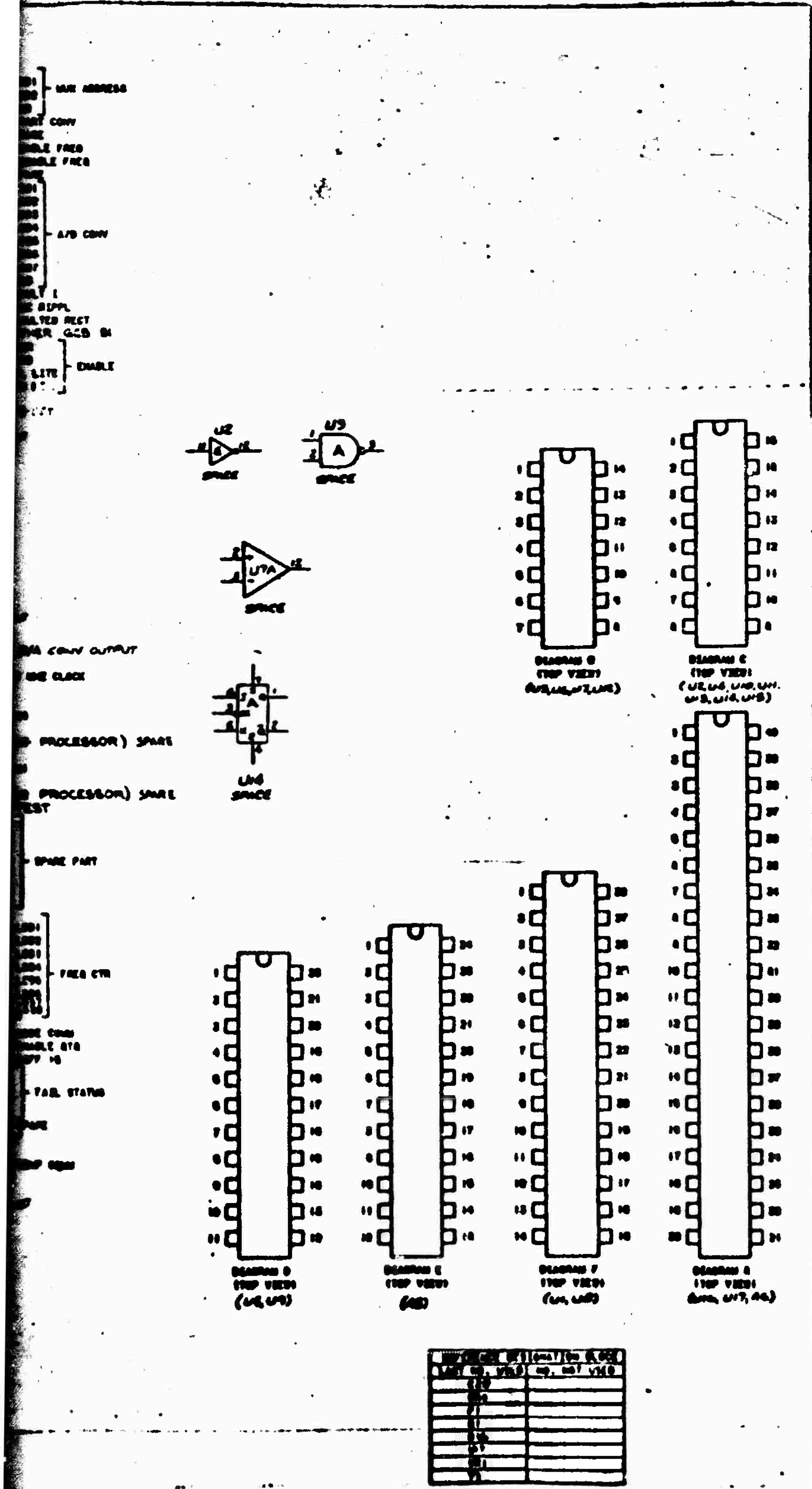


Figure 4-16

Schematic Wiring Diagram, Microprocessor and Memory Board, 2106389

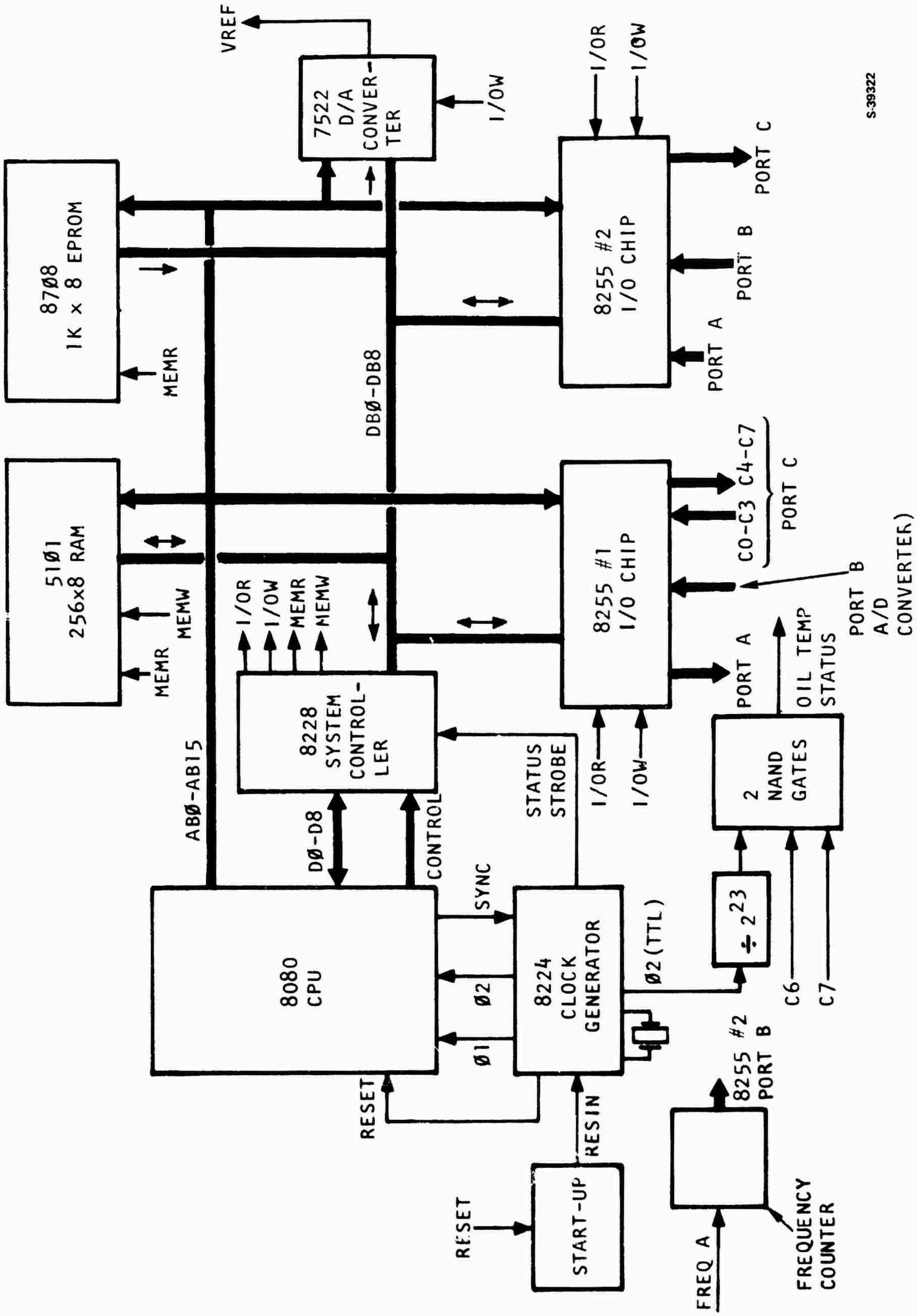


Figure 4-17. Microprocessor Board Block Diagram

generator with 1 KHz corresponding to 10,000 rpm. Chip U15 is a counter which will count the zero crossings of the sine wave over a period of time which is controlled by software through the two lines DISABLE FREQ and ENABLE FREQ. The software reads the final count and thus gets an indication of the speed of the generator.

Chips U12, U13, and U10 together form a counter which divides the Ø2 (TTL) clock by 2^{21}. Since the frequency of the Ø2 clock is 2.048 MHz, the output of the above-mentioned counter will be approximately a 1 Hz square wave. ENABLE FL LITE and ENABLE SS LITE are under software control. Depending on these two outputs, TEMP COMM will either be high or low or a 1 Hz square wave.

The AD7522 is a CMOS multiplying D/A converter with double buffered inputs. It is used to provide a reference voltage which determines the output of the 270 vdc generator. The control of the generator voltage is implemented on the I/O board, A3, and is discussed elsewhere in this report.

270V Generator Control Unit Software

General Description. The 270 vdc software is not interrupt driven. All timing information is derived from counting the number of clock cycles required to execute each and every instruction. The clock frequency is 2.048 MHz.

After initialization is completed and the generator is started, the software goes into a loop which takes 10 msec to be executed. While in this loop, the software reads different analog and digital inputs and makes decisions based on the values read. Thus each parameter is checked once every 10 msec.

The analog inputs monitored by the software are EO (bus voltage), POSI (current in the positive feeder), NEGI (current in the negative feeder), and TEMP (oil temperature). EO is used in the overvoltage and undervoltage tests, POSI is used in the overload tests, and both POSI and NEGI are used in feeder fault tests. TEMP is used in tests to determine whether an oil alarm signal should be output.

The I/O conditioning board conditions the ripple and ground current sensor output signals and produces two discrete outputs, one of ripple and another for ground current. A logic one on any of these lines indicates a fault condition on the corresponding input. Thus, as far as ripple fault and ground current fault are concerned, the 270 vdc GCU software monitors the state of discrete lines to determine the presence or absence of a fault.

A counter on the microprocessor board, A4, can be enabled and disabled under software control. When enabled, the counter is counting the zero crossings of one of the phases of the auxiliary winding. Consequently the counter output at the end of a count period will be proportional to the speed of the generator. The counter is allowed to count for a period of 100 msec; its output is read, the counter is reset and allowed to count for another 100 msec, and so on. Thus the speed of the generator is measured every 100 msec. A generator speed of 9000 rpm corresponds to a frequency of 900 Hz, which means that the counter will count to 90 if allowed to count for a period of 100 msec.

As mentioned earlier, it takes 10 msec for the software to execute one loop. A software counter, M1, is decremented by one each time the loop is executed once. When M1 reaches 0, the software goes out of the loop, stops the hardware counter, reads its output (which, as explained, corresponds to the speed of the generator), resets it, enables it, initializes M1 to 10 and returns to the 10 msec loop.

The flow chart (Figure 4-18) and the program listing (Figure 4-19) provide a complete representation of the software.

270 VDC GCU RAM Allocation

400H = 100 msec counter (M1)

402H = Least significant byte of 6 sec counter (MVLESS)

403H = Most significant byte of 6 sec counter (MVLESS)

404H = Least significant byte of 7 sec counter (MIMORE)

405H = Most significant byte of 7 sec counter (MIMORE)

406H - Least significant byte of 200 msec counter (MRIPPL)

407H = Most significant byte of 200 msec counter (MRIPPL)

408H = 200 msec counter (MVMORE)

410H = 20 msec counter (MGNDF)

411H = 20 msec counter (MFEEDR)

401H = Underspeed counter (MUSPED)

412H = POSI

413H = NEGI

414H = Least signficant byte of 100 X (POSI-NEGI)

415H = Most significant byte of 100 X (POSI-NEGI)

420H = VREF

421H = Undervoltage yes counter (UVYES)

422H = Undervoltage no counter (UVNO)

432H = Undervoltage flag (UNFLAG)

424H = Overload yes counter (OLYES)

425H = Overload no counter (OLNO)

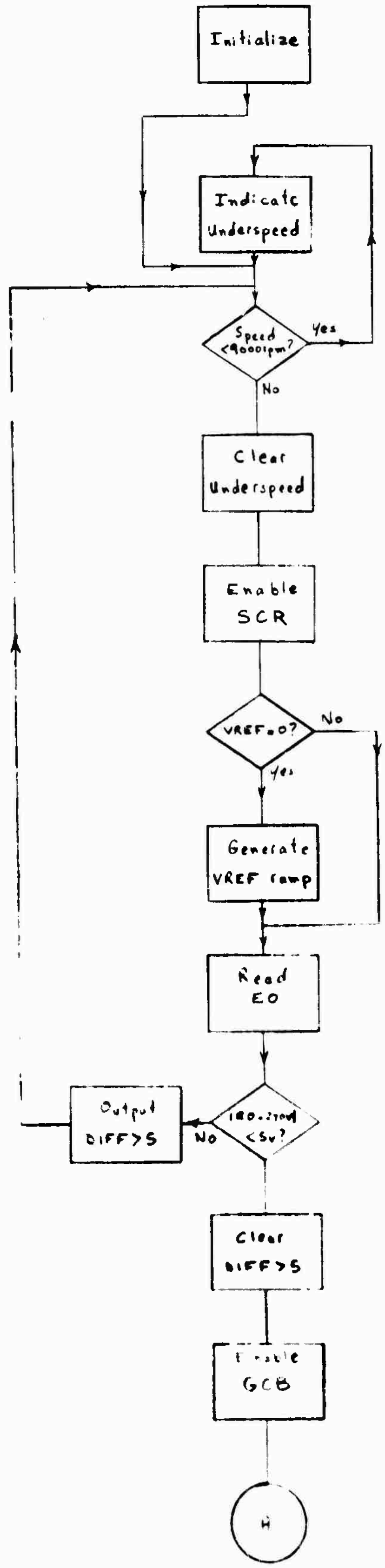


Figure 4-18. Microprocessor Flow Chart (1)

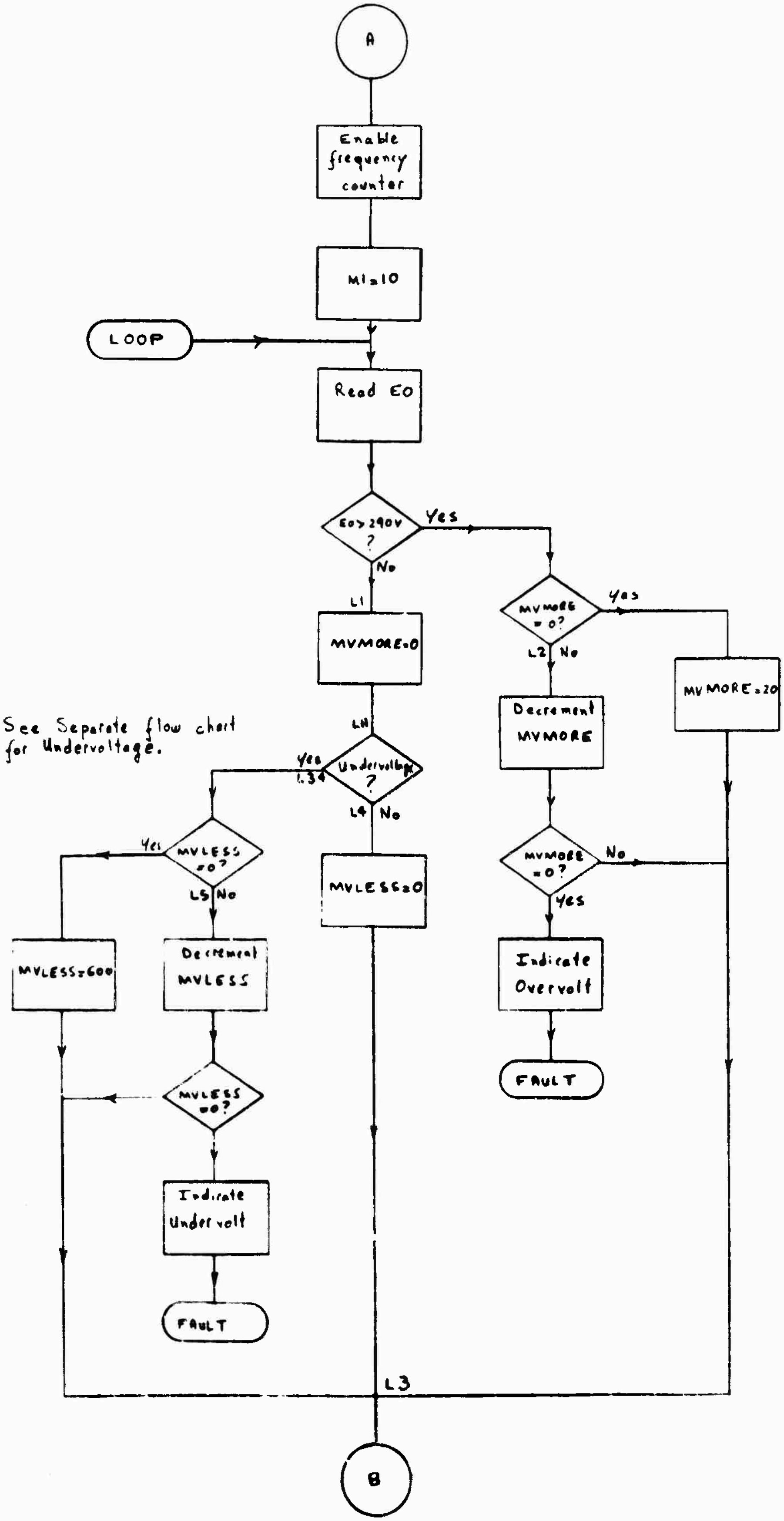


Figure 4-18. Microprocessor Flow Chart (2)

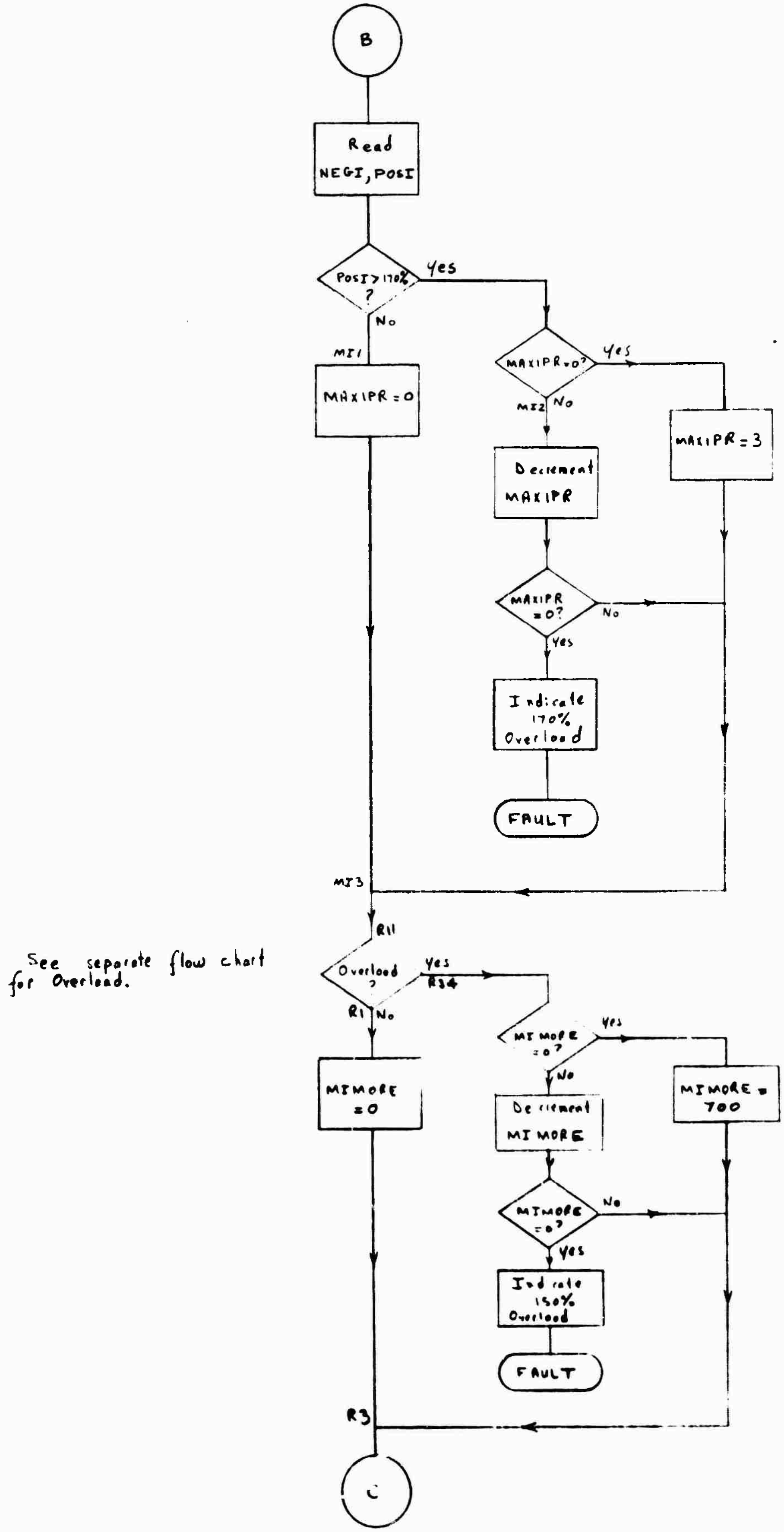


Figure 4-18. Microprocessor Flow Chart (3)

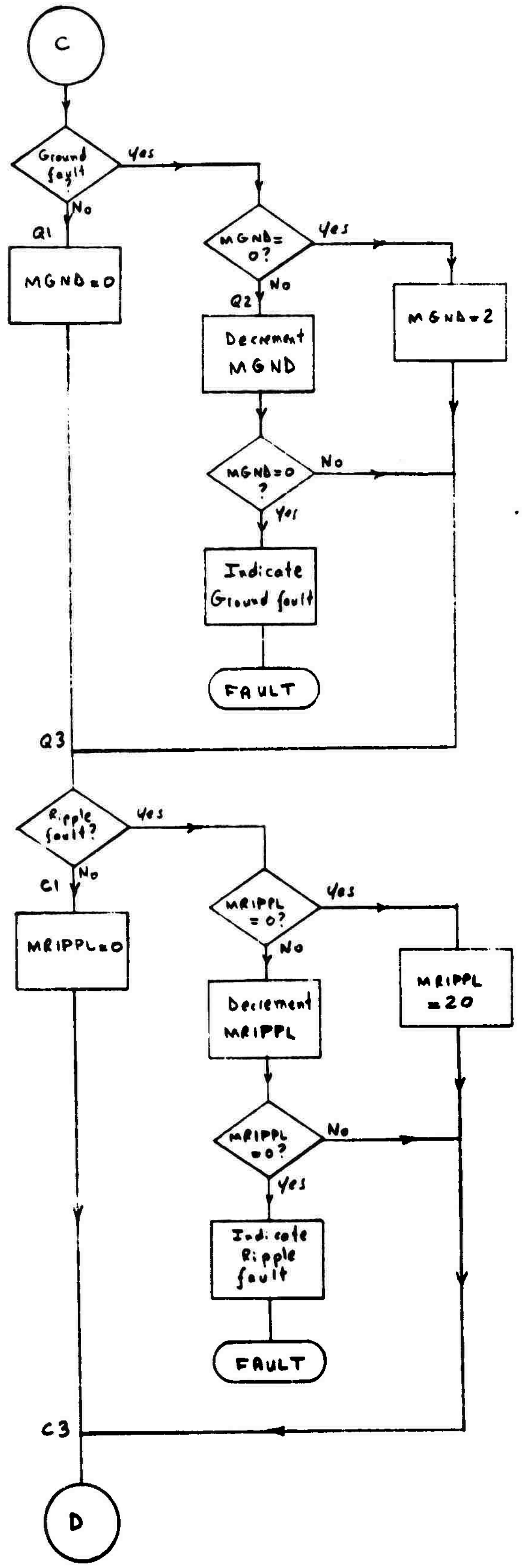


Figure 4-18. Microprocessor Flow Chart (4)

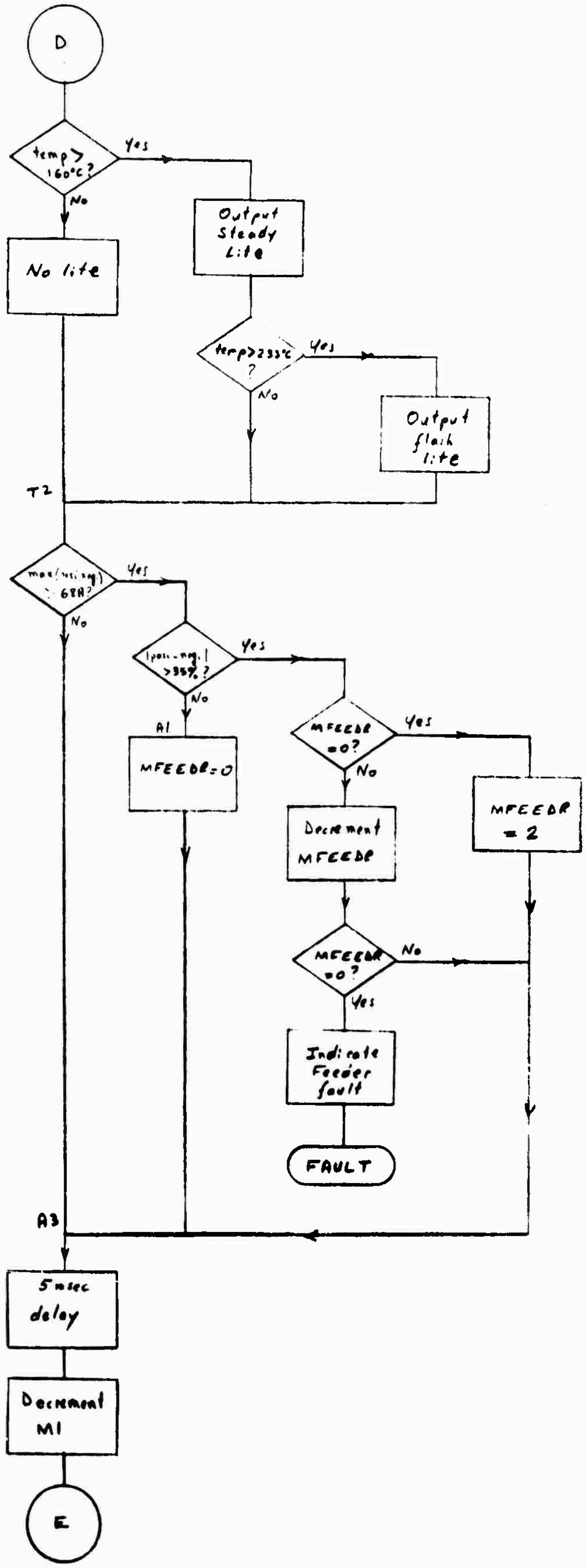


Figure 4-18. Microprocessor Flow Chart (5)

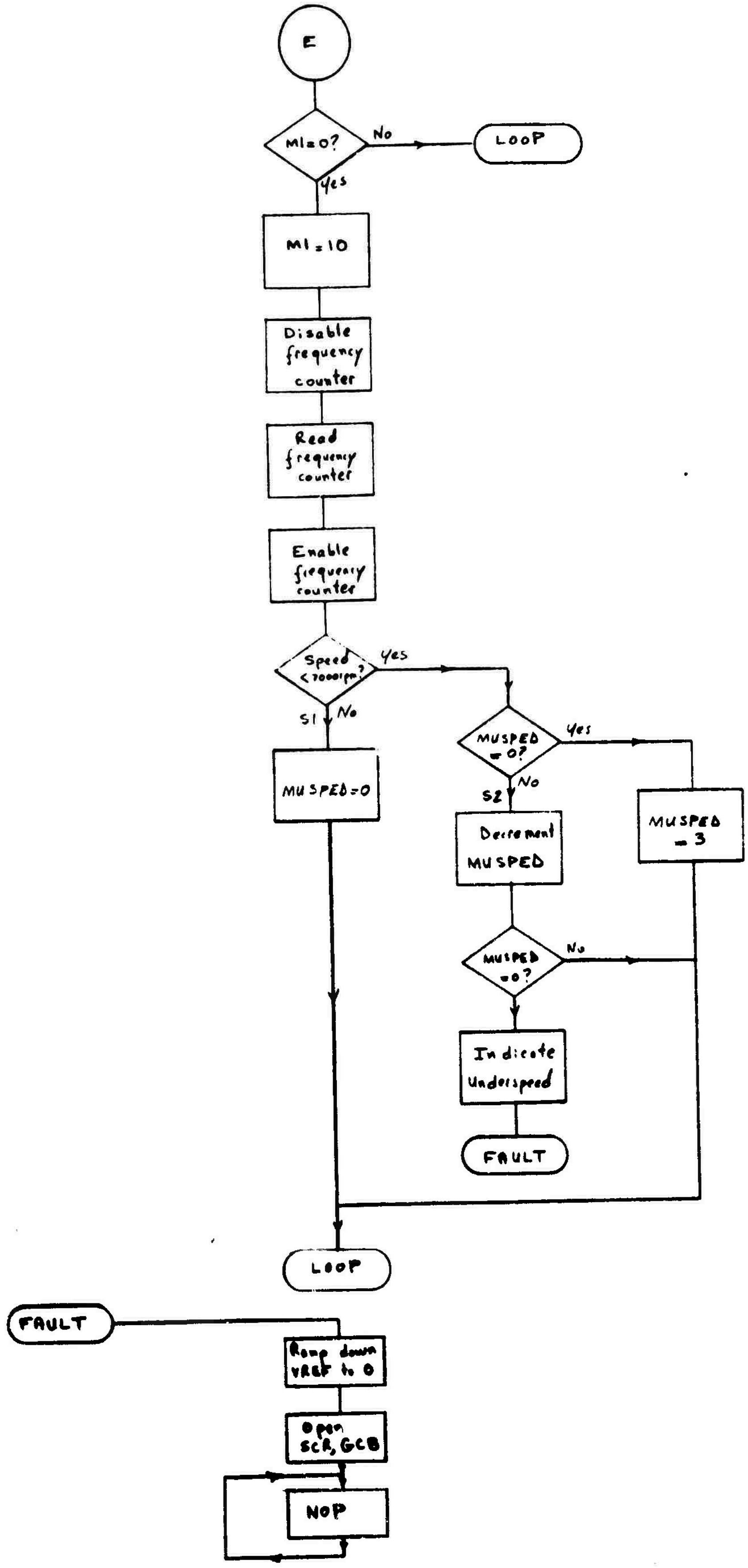
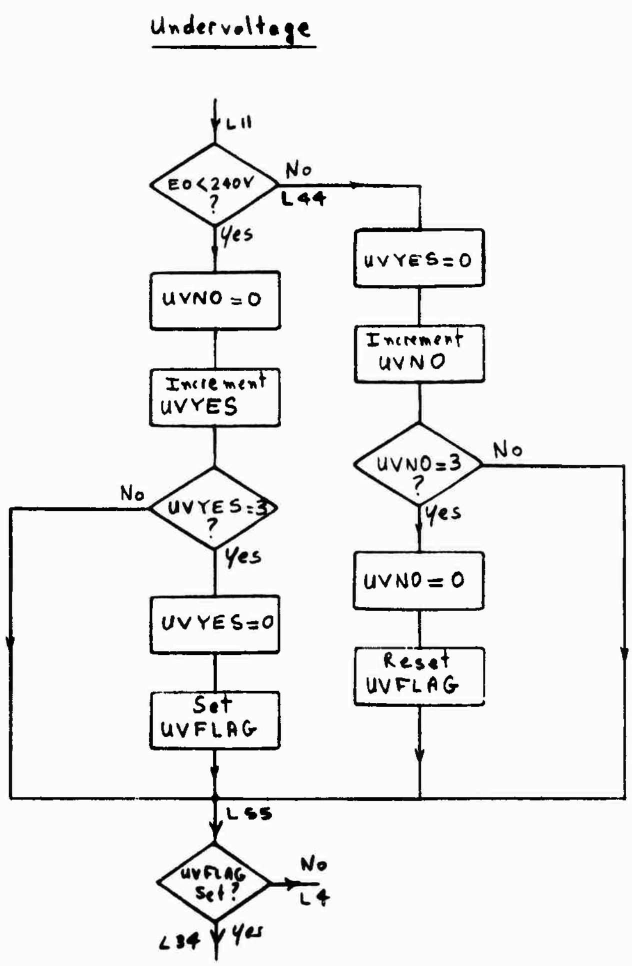


Figure 4-18. Microprocessor Flow Chart (6)



The above flow chart is equivalent to:

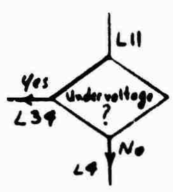
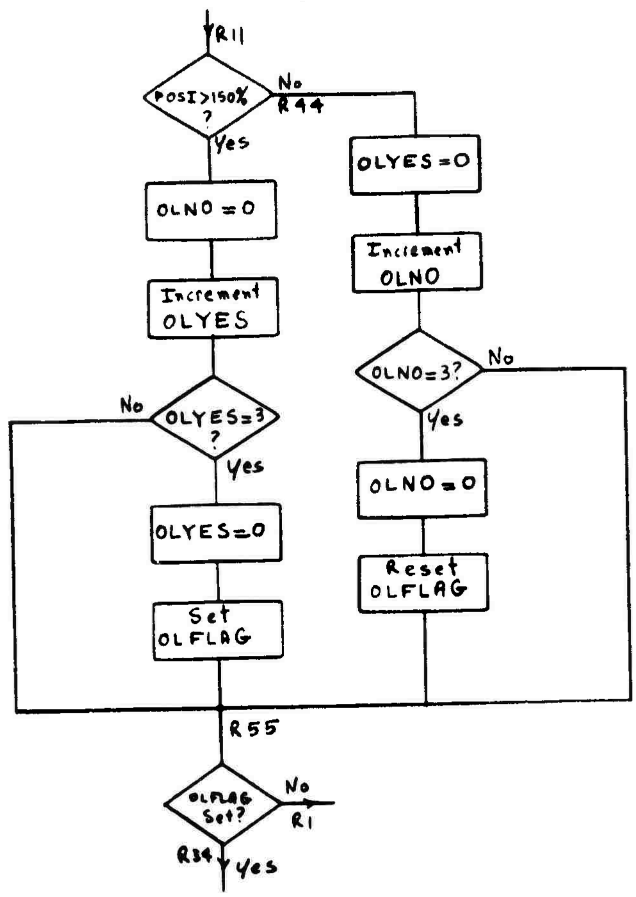


Figure 4-18. Microprocessor Flow Chart (7)

Overload



The above flow chart is equivalent to :

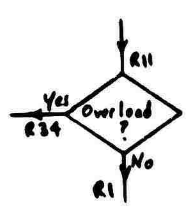


Figure 4-18. Microprocessor Flow Chart (8)

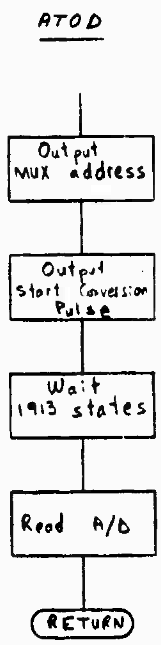


Figure 4-18. Microprocessor Flow Chart (9)

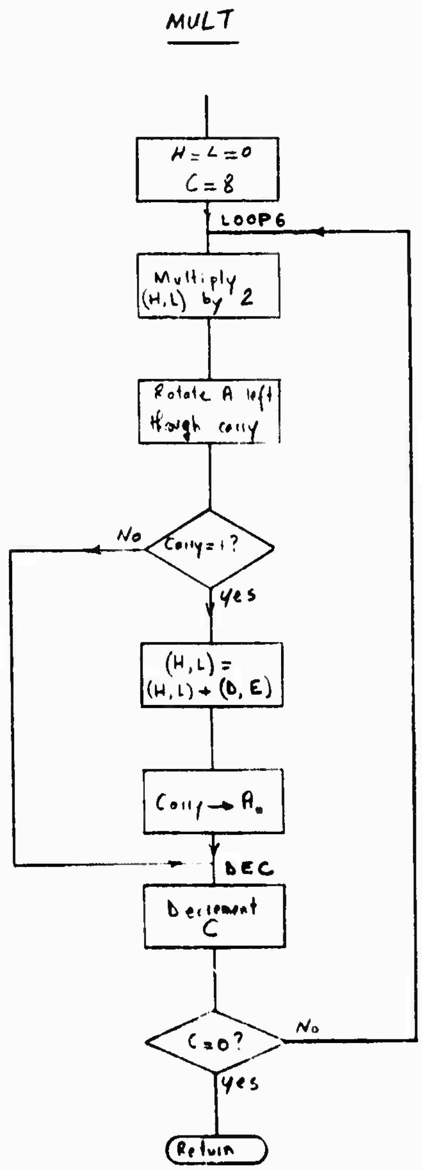


Figure 4-18. Microprocessor Flow Chart (10)

MICROKIT ASSEMBLER -- VER 2.1

```
0000                   ORG   X'050'
0050 F3         START  DI                 DISABLE INTERRUPT
                *INITIALIZE CONTROL WORDS OF I/O CHIPS
0051 3A7403            LDA   MOD1         CONF 8255 #1
0054 D30B              OUT   X'0B'
0056 3A7503            LDA   MOD2         CONF 8255 #2
0059 D313              OUT   X'13'
005B FB                EI
005C 31FF04            LXI   SP,X'4FF'    INITIALIXE
                *                         STACK POINTER
                *CLEAR ALL OUTPUT PORTS
005F 3E00              MVI   A,0
0061 D30A              OUT   X'0A'        DISAB GCB,SCR,TEMP
0063 D312              OUT   X'12'        CLR PORT C
0065 D308              OUT   X'08'        CLR PORT A
0067 D320              OUT   X'20'        D/A CONV=0
                *CLEAR RAM
0069 3EFF              MVI   A,255
006B 210004            LXI   H,X'400'
006E 3600       RAMF   MVI   M,0
0070 23                INX   H
0071 3D                DCR   A
0072 FE00              CPI   0
0074 C26E00            JNZ   RAMF
0077 C37E00            JMP   BEGIN
007A 3E30       UNSPD  MVI   A,X'30'
007C D312              OUT   X'12'        UNDERSPEED
007E 3E20       BEGIN  MVI   A,X'20'
0080 D308              OUT   X'08'        ENAB FREQ COUNTER
0082 3E00              MVI   A,0
0084 D308              OUT   X'08'
0086 0664              MVI   B,100
0088 3E64       LOOP1  MVI   A,100
008A 3D         LOOP2  DCR   A
008B 7F                MOV   A,A
008C C28A00            JNZ   LOOP2
008F C28A00            JNZ   LOOP2
0092 C28A00            JNZ   LOOP2
0095 05                DCR   B
0096 C28800            JNZ   LOOP1
0099 3E40              MVI   A,X'40'      DISAB FREQ COUNTER
009B D308              OUT   X'08'
009D 3E00              MVI   A,0
009F D308              OUT   X'08'
00A1 DB11              IN    X'11'        READ FREQ
00A3 FE5A              CPI   90           SPEED<9000 RPM?
00A5 DA7A00            JC    UNSPD
00A8 3E00              MVI   A,0          CLEAR UNDERSPEED
00AA D312              OUT   X'12'
00AC 3E10              MVI   A,X'10'      ENABLE SCR
00AE D30A              OUT   X'0A'
00B0 212004            LXI   H,X'420'
00B3 7E                MOV   A,M
00B4 FE00              CPI   0            VREF=0?
00B6 C2CC00            JNZ   NEX
00B9 3C         VREF   INR   A            START UP RAMP
00BA 0664              MVI   B,100
```

Figure 4-19. Microprocessor Program Listing (1)

MICROKIT ASSEMBLER -- VER 2.1

```
00BC 05      LOOP3  DCR  B
00BD 40             MOV  B,B
00BE C2BC00         JNZ  LOOP3
00C1 FE92           CPI  146        REF=270V?
00C3 D320           OUT  X'20'
00C5 DAB900         JC   VREF
00C8 212004         LXI  H,X'420'   STORE VREF IN
00CB 77             MOV  M,A        MEMORY
00CC 3E03    NEX    MVI  A,3        READ E0
00CE CD4403         CALL ATOD
00D1 47             MOV  B,A
00D2 3EE2           MVI  A,226      270V
00D4 4F             MOV  C,A
00D5 90             SUB  B          A=270V-EGEN
00D6 FADE00         JM   EXCH1
00D9 FE04           CPI  4          5.54 VOLTS
00DB C3E200         JMP  ENABL
00DE 78      EXCH1  MOV  A,B
00DF 91             SUB  C          A=EGEN-270V
00E0 FE04           CPI  4
00E2 DAEC00  ENABL  JC   GCB
00E5 3E04           MVI  A,X'04'
00E7 D312           OUT  X'12'      DIFF>5V
00E9 C37E00         JMP  BEGIN
00EC 3E00    GCB    MVI  A,0
00EE D312           OUT  X'12'      CLR DIIF>5
00F0 3E30           MVI  A,X'30'
00F2 D30A           OUT  X'0A'      GCB ENABLE
00F4 3E20           MVI  A,X'20'    ENABLE FREQ CNTR
00F6 D308           OUT  X'08'
00F8 3E00           MVI  A,0
00FA D308           OUT  X'08'
00FC 210004         LXI  H,X'400'
00FF 360A           MVI  M,10       M1=10
0101 3E03    LOOP   MVI  A,3        READ E0
0103 CD4403         CALL ATOD
0106 FEF2           CPI  242        E0>290V?
0108 210804         LXI  H,X'408'   MVMORE
010B DA2701         JC   L1
010E 7E             MOV  A,M
010F FE00           CPI  0          MVMORE=0?
0111 C21901         JNZ  L2
0114 3614           MVI  M,20       MVMORE=20; 200MSEC
0116 C39301         JMP  L3
0119 3D      L2     DCR  A
011A 77             MOV  M,A
011B FE00           CPI  0
011D C29301         JNZ  L3
0120 3E38           MVI  A,X'38'    INDICATE OVERVOLT
0122 D312           OUT  X'12'
0124 C32903         JMP  FAULT
0127 3600    L1     MVI  M,0        MVMORE=0
0129 FEC9           CPI  201        E0<240V?
012B D24701         JNC  L44
012E 212204         LXI  H,X'422'
0131 3600           MVI  M,0        UVNO=0
0133 212104         LXI  H,X'421'
```

Figure 4-19. Microprocessor Program Listing (2)

MICROKIT ASSEMBLER -- VER 2.1

```
0136 34              INR  M          UVYES=UVYES+1
0137 7E              MOV  A,M
0138 FE03            CPI  3
013A C25D01          JNZ  L55
013D 3600            MVI  M,0
013F 212304          LXI  H,X'423'
0142 3601            MVI  M,1        SET UVFLAG
0144 C35D01          JMP  L55
0147 212104 L44      LXI  H,X'421'
014A 3600            MVI  M,0
014C 212204          LXI  H,X'422'
014F 34              INR  M
0150 7E              MOV  A,M
0151 FE03            CPI  3
0153 C25D01          JNZ  L55
0156 3600            MVI  M,0
0158 212304          LXI  H,X'423'
015B 3600            MVI  M,0
015D 212304 L55      LXI  H,X'423'
0160 7E              MOV  A,M
0161 FE00            CPI  0
0163 CA8D01          JZ   L4
0166 2A0204          LHLD X'402'     (H,L)=MVLESS
0169 7C              MOV  A,H
016A 85              ADD  L          A=H+L
016B C27A01          JNZ  L5
016E DA7A01          JC   L5
0171 215802          LXI  H,600      MVLESS=600
0174 220204          SHLD X'402'
0177 C39301          JMP  L3
017A 2B      L5      DCX  H          DECREMENT MVLESS
017B 220204          SHLD X'402'
017E 7C              MOV  A,H
017F 85              ADD  L          A=H+L
0180 C29301          JNZ  L3
0183 DA9301          JC   L3
0186 3E40            MVI  A,X'40'    INDICATE UNDERVOLT
0188 D312            OUT  X'12'
018A C32903          JMP  FAULT
018D 210000 L4       LXI  H,0        MVLESS=0
0190 220204          SHLD X'402'
0193 3E05    L3      MVI  A,5        READ NEGI
0195 CD4403          CALL ATOD
0198 211304          LXI  H,X'413'
019B 77              MOV  M,A        STORE NEGI
019C 3E04            MVI  A,4        READ POSI
019E C37603          JMP  PATCH1
01A1 00              NOP
01A2 7E      L3P     MOV  A,M
01A3 FED3            CPI  211        POSI>150%?
01A5 DAC101          JC   R44
01A8 212504          LXI  H,X'425'
01AB 3600            MVI  M,0
01AD 212404          LXI  H,X'424'
01B0 34              INR  M
01B1 7E              MOV  A,M
01B2 FE03            CPI  3
```

Figure 4-19. Microprocessor Program Listing (3)

```
MICROKIT ASSEMBLER -- VER 2.1

01B4 C2D701          JNZ  R55
01B7 3600            MVI  M,0
01B9 212604          LXI  H,X'426'
01BC 3601            MVI  M,1
01BE C3D701          JMP  R55
01C1 212404 R44      LXI  H,X'424'
01C4 3600            MVI  M,0
01C6 212504          LXI  H,X'425'
01C9 34              INR  M
01CA 7E              MOV  A,M
01CB FE03            CPI  3
01CD C2D701          JNZ  R55
01D0 3600            MVI  M,0
01D2 212604          LXI  H,X'426'
01D5 3600            MVI  M,0
01D7 212604 R55      LXI  H,X'426'
01DA 7E              MOV  A,M
01DB FE00            CPI  0
01DD CA0702          JZ   R1
01E0 2A0404          LHLD X'404'     (H,L)=MIMORE
01E3 7C              MOV  A,H
01E4 85              ADD  L          A=H+L
01E5 C2F401          JNZ  R5
01E8 DAF401          JC   R5
01EB 21BC02          LXI  H,700      MIMORE=700
01EE 220404          SHLD X'404'
01F1 C30D02          JMP  R3
01F4 2B      R5      DCX  H          DECREMENT MIMORE
01F5 220404          SHLD X'404'
01F8 7C              MOV  A,H
01F9 85              ADD  L          A=H+L
01FA C20D02          JNZ  R3
01FD DA0D02          JC   R3
0200 3E10            MVI  A,X'10'    INDICATE OVERLOAD
0202 D312            OUT  X'12'
0204 C32903          JMP  FAULT
0207 210000 R1       LXI  H,0
020A 220404          SHLD X'404'     MIMORE=0
020D DB0A    R3      IN   X'0A'
020F 0F              RRC
0210 211004          LXI  H,X'410'
0213 47              MOV  B,A
0214 D23002          JNC  Q1
0217 7E              MOV  A,M
0218 FE00            CPI  0          MGND=0?
021A C22202          JNZ  Q2
021D 3602            MVI  M,2        MGND=2
021F C33202          JMP  Q3
0222 3D      Q2      DCR  A
0223 77              MOV  M,A
0224 FE00            CPI  0
0226 C23202          JNZ  Q3
0229 3E20            MVI  A,X'20'    GROUND FAULT
022B D312            OUT  X'12'
022D C32903          JMP  FAULT
0230 3600    Q1      MVI  M,0        MGND=0
0232 78      Q3      MOV  A,B
```

Figure 4-19. Microprocessor Program Listing (4)

MICROKIT ASSEMBLER -- VER 2.1

```
0233 0F                RRC
0234 D25E02            JNC  C1
0237 2A0604            LHLD X'406'     MRIPPL
023A 7C                MOV  A,H
023B 85                ADD  L          A=H+L
023C C24B02            JNZ  C2
023F DA4B02            JC   C2
0242 211400            LXI  H,20
0245 220604            SHLD X'406'     MRIPPL=20
0248 C36402            JMP  C3
024B 2B         C2     DCX  H          DECREMENT MRIPPL
024C 220604            SHLD X'406'
024F 7C                MOV  A,H
0250 85                ADD  L
0251 C26402            JNZ  C3
0254 DA6402            JC   C3
0257 3E18              MVI  A,X'18'    RIPPLE FAULT
0259 D312              OUT  X'12'
025B C32903            JMP  FAULT
025E 210000     C1     LXI  H,0
0261 220604            SHLD X'406'     MRIPPL=0
0264 3E01       C3     MVI  A,1        READ TEMP
0266 CD4403            CALL ATOD
0269 47                MOV  B,A
026A FE7E              CPI  126        TEMP>160C?
026C D28002            JNC  T1
026F 3EB0              MVI  A,X'B0'    OUTPUT SS LITE
0271 D30A              OUT  X'0A'
0273 78                MOV  A,B
0274 FE22              CPI  34         TEMP>233?
0276 D28402            JNC  T2
0279 3EF0              MVI  A,X'F0'    OUTPUT FL LITE
027B D30A              OUT  X'0A'
027D C38402            JMP  T2
0280 3E30       T1     MVI  A,X'30'    NO LITE
0282 D30A              OUT  X'0A'
0284 211304     T2     LXI  H,X'413'
0287 4E                MOV  C,M        C=NEGI
0288 2B                DCX  H
0289 7E                MOV  A,M        A=POSI
                *A=MAX(POSI,NEGI);C=MIN(POSI,NEGI)
028A B9                CMP  C
028B D29102            JNC  A4
028E 57                MOV  D,A
028F 79                MOV  A,C
0290 4A                MOV  C,D
0291 FE3A       A4     CPI  58         I<68A?
0293 DAD002            JC   A3
0296 47                MOV  B,A        B=MAX
0297 91                SUB  C          A=DIFFERENCE
0298 1600              MVI  D,0
029A 1E64              MVI  E,100
029C CD6203            CALL MULT       100XDIFF
029F 221404            SHLD X'414'
02A2 1600              MVI  D,0
02A4 1E23              MVI  E,35
02A6 78                MOV  A,B
```

Figure 4-19. Microprocessor Program Listing (5)

MICROKIT ASSEMBLER -- VER 2.1

```
02A7 CD6203          CALL  MULT         35XMAX
02AA 7C              MOV   A,H          A=MOST SIG BYTE
                                        OF 35XMAX
02AB 211504          LXI   H,X'415'
02AE BE              CMP   M            35XMAX>100XDIFF?
02AF 211104          LXI   H,X'411'     MFEEDR
02B2 D2CE02          JNC   A1
02B5 7E              MOV   A,M
02B6 FE00            CPI   0
02B8 C2C002          JNZ   A2
02BB 3602            MVI   M,2
02BD C3D002          JMP   A3
02C0 3D        A2    DCR   A
02C1 77              MOV   M,A
02C2 FE00            CPI   0
02C4 C2D002          JNZ   A3
02C7 3E09            MVI   A,X'09'      INDICATE FEEDR FAU
02C9 D312            OUT   X'12'
02CB C32903          JMP   FAULT
02CE 3600      A1    MVI   M,0          MFEEDR=0
02D0 0605      A3    MVI   B,5
02D2 3E64      LOP1  MVI   A,100
02D4 3D        LOP2  DCR   A
02D5 7F              MOV   A,A
02D6 C2D402          JNZ   LOP2
02D9 C2D402          JNZ   LOP2
02DC C2D402          JNZ   LOP2
02DF 05              DCR   B
02E0 C2D202          JNZ   LOP1
02E3 210004          LXI   H,X'400'
02E6 35              DCR   M
02E7 7E              MOV   A,M
02E8 FE00            CPI   0
02EA C20101          JNZ   LOOP
02ED 360A            MVI   M,10         M1=10
02EF 3E40            MVI   A,X'40'      DISABLE FREQ CNTR
02F1 D308            OUT   X'08'
02F3 3E00            MVI   A,0
02F5 D308            OUT   X'08'
02F7 DB11            IN    X'11'        READ SPEED
02F9 47              MOV   B,A
02FA 3E20            MVI   A,X'20'      ENABLE FREQ CNTR
02FC D308            OUT   X'08'
02FE 3E00            MVI   A,0
0300 D308            OUT   X'08'
0302 78              MOV   A,B
0303 FE46            CPI   70           SPEED<7000RPM?
0305 210104          LXI   H,X'401'     MUSPED
0308 D22403          JNC   S1
030B 7E              MOV   A,M
030C FE00            CPI   0
030E C21603          JNZ   S2
0311 3603            MVI   M,3
0313 C30101          JMP   LOOP
0316 3D        S2    DCR   A
0317 77              MOV   M,A
0318 FE00            CPI   0
```

Figure 4-19. Microprocessor Program Listing (6)

MICROKIT ASSEMBLER -- VER 2.1

```
031A C20101          JNZ   LOOP
031D 3E30            MVI   A,X'30'    INDICATE UNDERSPED
031F D312            OUT   X'12'
0321 C32903          JMP   FAULT
0324 3600     S1     MVI   M,0
0326 C30101          JMP   LOOP
0329 3E6C     FAULT  MVI   A,108
032B 3D       PHASBK DCR   A
032C 47              MOV   B,A
032D 1607            MVI   D,7        WAIT  .092MSEC
032F 15       LOOP4  DCR   D
0330 52              MOV   D,D
0331 C22F03          JNZ   LOOP4
0334 78              MOV   A,B
0335 FE00            CPI   0
0337 D320            OUT   X'20'
0339 C22B03          JNZ   PHASBK
033C 3E00            MVI   A,0        OPEN SCR,GCB
033E D30A            OUT   X'0A'
0340 00       TERM   NOP
0341 C34003          JMP   TERM
              ****************************************
              *
              * SUBROUTINE ATOD IS USED TO READ ONE
              *OF THE 8 CHANNELS OF THE ANALOG
              *MULTIPLEXER.AS AN INPUT TO THIS ROUTINE
              *THE ACCUMULATOR MUST CONTAIN THE
              *ADDRESS(IN INVERTED FORM) OF THE
              *PROPER CHANNEL.THE ROUTINE RETURNS THE
              *RESULT IN THE ACCUMULATOR
              *
0344 2F       ATOD   CMA                  COMP ACCUM
0345 D6F8            SUI   X'F8'
0347 D308            OUT   X'08'      OUTPUT ADDRESS
0349 00              NOP
034A 00              NOP
034B 00              NOP
034C 00              NOP
034D 00              NOP
034E 00              NOP
              *
              *
              * START CONVERSION PULSE
              *
034F C608            ADI   8
0351 D308            OUT   X'08'
0353 D608            SUI   8
0355 D308            OUT   X'08'
              *
              * WAIT 1 MSEC
              *
0357 3E64            MVI   A,100      A=100
0359 57              MOV   D,A
035A 15       LOOP5  DCR   D
035B 00              NOP
035C C25A03          JNZ   LOOP5
              *
```

Figure 4-19. Microprocessor Program Listing (7)

MICROKIT ASSEMBLER -- VER 2.1

```
035F DB09          IN    X'09'      READ A/D
0361 C9            RET
```

Figure 4-19. Microprocessor Program Listing (8)

```
MICROKIT ASSEMBLER -- VER 2.1

                     *
                     ***************************************
                     *
                     * SUBROUTINE MULT MULTIPLIES AN 8 BIT
                     *NUMBER(IN A) WITH A 16 BIT NUMBER
                     *IN REGISTERS D AND E.THE MOST SIG.
                     *BYTE OF THE RESULT IS RETURNED IN H
                     *AND THE LEAST SIG. BYTE IN L
                     *
0362 210000 MULT     LXI   H,0
0365 0E08            MVI   C,8
0367 29     LOOP6    DAD   H
0368 17              RAL
0369 D26F03          JNC   DEC
036C 19              DAD   D
036D CE00            ACI   0
036F 0D     DEC      DCR   C
0370 C26703          JNZ   LOOP6
0373 C9              RET


0374 83     MOD1     DC    X'83'
0375 92     MOD2     DC    X'92'
0376 CD4403 PATCH1   CALL  ATOD
0379 2B              DCX   H
037A 77              MOV   M,A
037B FEEF            CPI   239
037D 213004          LXI   H,X'430'
0380 DA9C03          JC    MI1
0383 7E              MOV   A,M
0384 FE00            CPI   0
0386 C28E03          JNZ   MI2
0389 3603            MVI   M,3
038B C39E03          JMP   MI3
038E 3D     MI2      DCR   A
038F 77              MOV   M,A
0390 FE00            CPI   0
0392 C29E03          JNZ   MI3
0395 3E78            MVI   A,X'78'
0397 D312            OUT   X'12'
0399 C32903          JMP   FAULT
039C 3600   MI1      MVI   M,0
039E 211204 MI3      LXI   H,X'412'
03A1 C3A201          JMP   L3P
03A4                 END   START
```

Figure 4-19. Microprocessor Program Listing (9)

MICROKIT ASSEMBLER -- VER 2.1

B	0000	C	0001	D	0002	E	0003
H	0004	L	0005	M	0006	A	0007
SP	0006	PSW	0006	START	0050	RAMF	006E
UNSPD	007A	BEGIN	007E	LOOP1	0088	LOOP2	008A
VREF	00B9	LOOP3	00BC	NEX	00CC	EXCH1	00DE
ENABL	00E2	GCB	00EC	LOOP	0101	L2	0119
L1	0127	L44	0147	L55	015D	L5	017A
L4	018D	L3	0193	L3P	01A2	R44	01C1
R55	01D7	R5	01F4	R1	0207	R3	020D
Q2	0222	Q1	0230	Q3	0232	C2	024B
C1	025E	C3	0264	T1	0280	T2	0284
A4	0291	A2	02C0	A1	02CE	A3	02D0
LOP1	02D2	LOP2	02D4	S2	0316	S1	0324
FAULT	0329	PHASBK	032B	LOOP4	032F	TERM	0340
ATOD	0344	LOOP5	035A	MULT	0362	LOOP6	0367
DEC	036F	MOD1	0374	MOD2	0375	PATCH1	0376
MI2	038E	MI1	039C	MI3	039E		

Figure 4-19. Microprocessor Program Listing (10)

426H = Overload flag (OLFLAG)

430H = 30 msec counter (MAXIPR)

270 VDC GCU I/O Configuration

8255 No. 1

(1) Output Port A (address = 08H)

PA7 : Spare
PA6 : Disable frequency counter
PA5 : Enable frequency counter
PA4 : Spare
PA3 : Start A/D conversion
PA2 : Most significant bit of MUX address
PA1 : Middle bit of MUX address
PA0 : Least significant bit of MUX address

(2) Input Port B (address = 09H)

The A/D converter output is connect to port B with the most significant bit tied to PB7 and the least significant bit tied to PB0

(3) Port C (address = 0AH)

PC7 : Steady-state light (output)
PC6 : Flashing light (output)
PC5 : GCB enable (output)
PC4 : SCR enable (output)
PC3 : Other GCB B1 (input)
PC2 : Faulted rectifier (input)
PC1 : Excess ripple fault (input)
PC0 : Ground current fault (input)

(4) Control Port (address = 0BH)

The initialization routine writes 83H into the control port.

8255 No. 2

(1) Input Port A (address = 10H)

PA7 : Spare
PA6 : Spare
PA5 : Spare
PA4 : Spare
PA3 : Spare
PA2 : Spare
PA1 : Spare
PA0 : State of TEST switch

(2) Input Port B (address = 11H)

The frequency counter output is connected to port B with the most significant bit tied to PB7 and the least significant bit tied to PB0.

(3) Output Port C (address = 12H)

PC7 : Spare
PC6 : Fail status 4 (F4)
PC5 : Fail status 3 (F3)
PC4 : Fail status 2 (F2)
PC3 : Fail status 1 (F1)
PC2 : DIFF 5
PC1 : Enable BTB
PC0 : Mode command

(4) Control Port (address = 13H)

The initialization routine writes 92H into the control port.

Fault Monitoring As can be seen from the flow chart (Figure 4-18), the basic function of the 270 vdc GCU software is to monitor different parameters related to the operation of the generator and to shut down the unit in case a fault condition is detected. The software will also provide a digital code on the lines F1, F2, F3, F4 to indicate the nature of the fault. Table 4-10 summarizes the different faults and the corresponding output codes.

TABLE 4-10. FAULT SUMMARY AND CODES

F4	F3	F2	F1	Fault
0	0	0	0	No fault
0	0	0	1	POSI/NEGI 35%, 30 msec
0	0	1	0	POSI 150%, 7 sec
0	0	1	1	Ripple 24 v p-p, 200 msec
0	1	0	0	Ground current 5 ma, 30 msec
0	1	1	0	Speed 7000 rpm, 400 msec
1	0	0	0	EO 240 v, 6 sec
0	1	1	1	EO 290 v, 200 msec
1	1	1	1	POSI 170%, 40 msec

Filtering of Monitored Parameters To eliminate nuisance tripping of the generator because of noise spikes on inputs monitored by the microprocessor, a minimum number of consecutive readings must indicate the presence of a fault before a fault is actually indicated by the processor and the unit is shut down. For example, a ground fault will be indicated if the software reads four consecutive readings equivalent to the ground current being greater than 5 ma. The flow chart shows the number of readings required for other inputs before a fault condition is actually indicated. The following paragraphs examine overload and undervoltage faults where a more complicated scheme of software filtering is required.

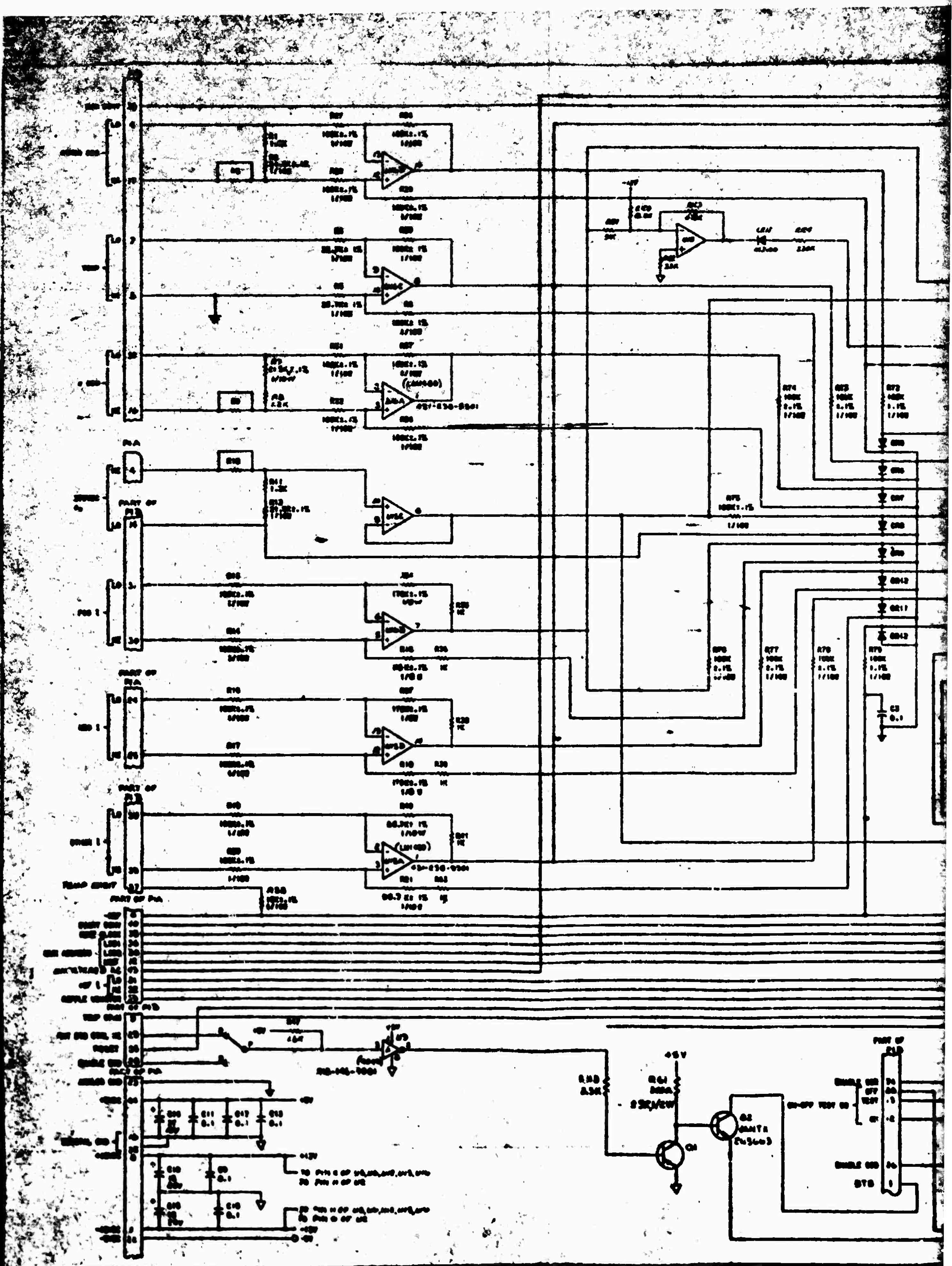
The spec requires the generator to be shut down if the current exceeds 150 percent of nominal current for a duration of 7 seconds. Since the duration of the basic loop is 10 msec, a total of 700 consecutive readings of POSI > 150% would correspond to an overload condition of 7 seconds. The problem with this method is that the unit might actually never trip even though an overload condition exists for 7 seconds or longer, the reason being that a spike on the POSI input might cause one reading POSI < 150% and reset the overload fault counter, MIMORE.

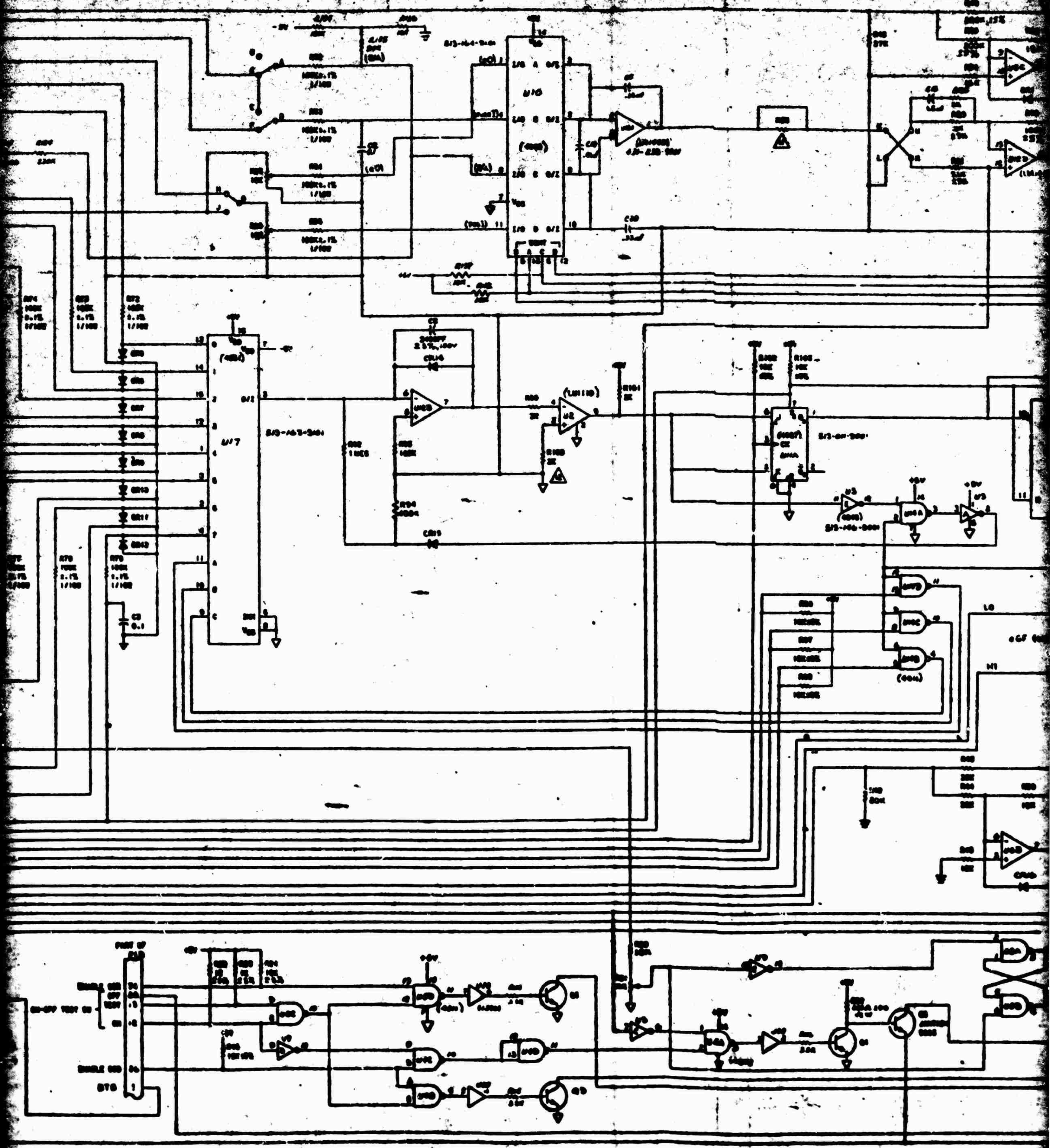
For this reason a different criterion is followed to determine whether the overload fault counter should be reset to zero or allowed to count down. This is best illustrated on the eighth page of the flow chart, titled "Overload". The basic idea is that an overload flag, OLFLAG, will be set if three consecutive readings indicate POSI > 150% and the overload flag will be reset if three consecutive readings indicate POSI < 150%. A similiar procedure is followed for undervoltage tests.

Oil Temperature Monitoring If the generator oil temperature exceeds 160°C, a steady light should be indicated in the cockpit. Above 233°C, the light should be flashing. The microprocessor controls two discrete outputs provided for this purpose. These are bit 7 and bit 6 of Port C of 8255 No. 1 (refer to the description of the I/O configuration). For temperatures less than 160°C both of these bits are logic zero. For temperatures between 160°C and 233°C, bit 7 is logic one and bit 6 is logic zero. For temperatures higher than 233°C, both bits are logic one. The hardware decodes these two discrete outputs to produce no light, a steady light, or a flashing light.

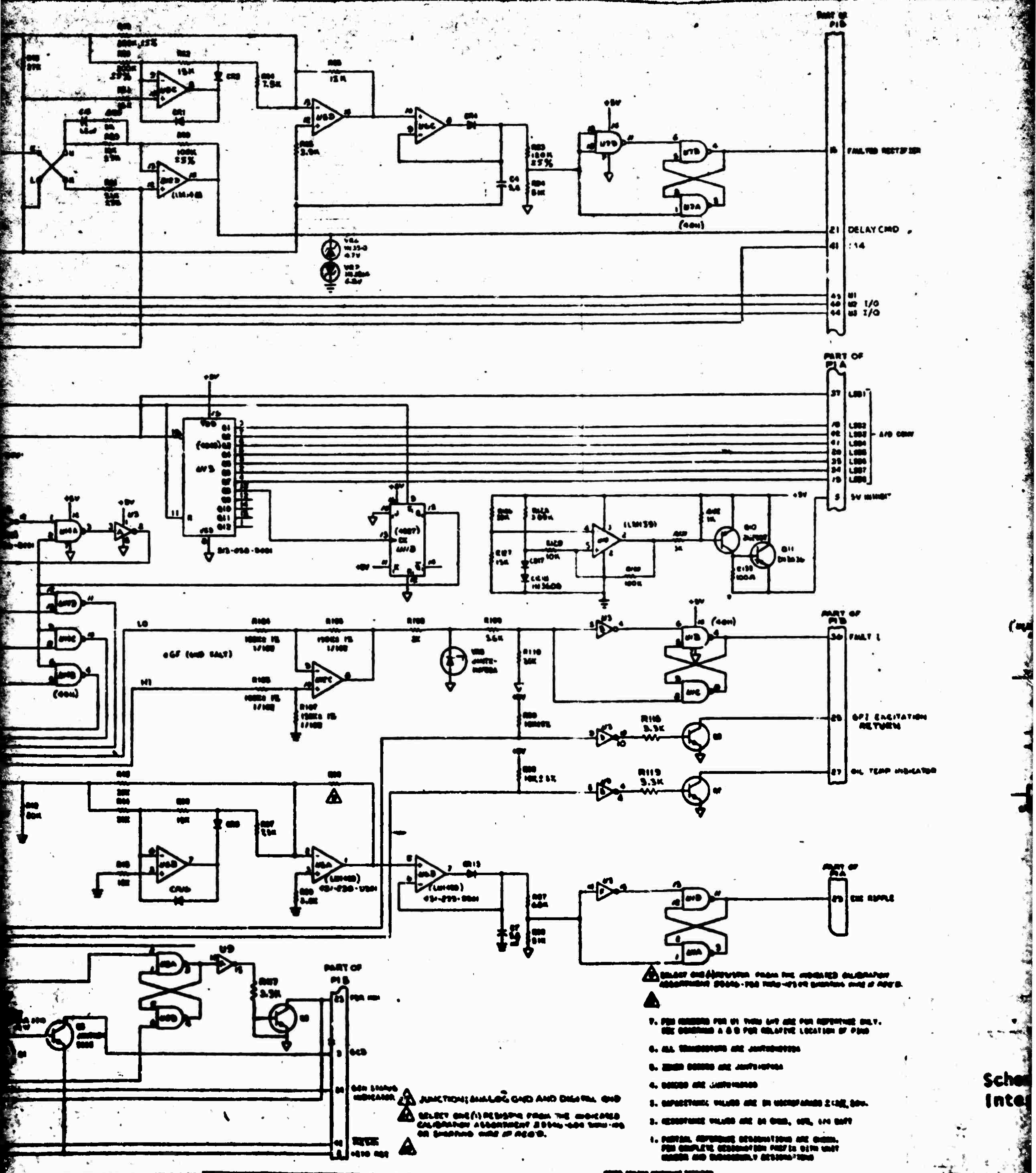
Input/Output (I/O) Interface Drawing 2106399 (Figure 4-20) shows the schematic of the I/O interface board. This board conditions input signals and provides drivers for output signals. The voltage regulator is also on this board, and is discussed elsewhere.

The analog signals which are brought to this board are first buffered and multiplied by a gain factor. After that they go to an analog multiplexer which lets one of them through, depending on its address input which is under microprocessor control. The output of the multiplexer goes to an A/D converter whose output can be read by the microprocessor. Table 4-11 provides a list of all the analog inputs and traces them all the way up to the A/D converter output.





2


FAILED RECTIFIER
DELAY CMD
PART OF P1A
A/D CONV
5V INHIBIT
FAULT 1
OIL TEMP INDICATOR
JUNCTION; ANALOG GND AND DIGITAL GND

13

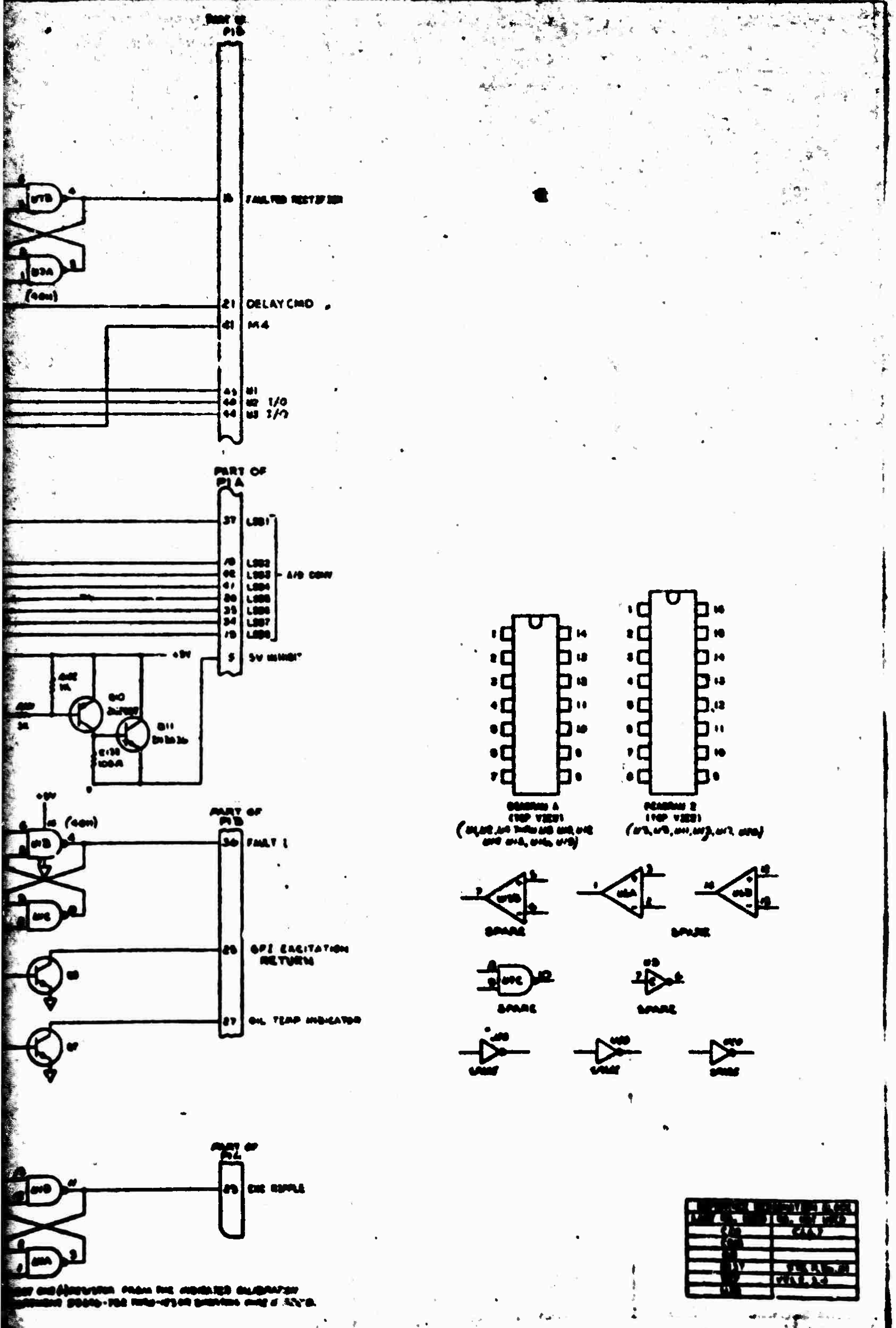


Figure 4-20

Schematic Wiring Diagram, I/O Interface Board, 2106399

TABLE 4-11. ANALOG CHANNELS

MUX	Channel	V input (volts)	V buffered volts)	A/D output (decimal)	Condition
0	OTHER GEN	100 240 270 290	2.647 6.352 7.146 7.675	75 181 203 218	 Undervolt Nominal Overvolt
1	TEMP	-1.050 -0.281	4.430 1.185	126 34	160°C 233°C
2	EGEN (Generator Terminals)	100 240 270 290	2.647 6.352 7.146 7.675	75 181 203 218	 Undervolt Nominal Overvolt
3	270VDC EO (Point of Regulation)	100 240 270 290	2.938 7.050 7.932 8.519	84 201 226 242	 Undervolt Nominal Overvolt
4	POSI	1.133 2.767 4.150	2.029 4.952 7.428	58 141 211	68A Nominal (166A) 150% (249A)
5	NEGI	1.133 2.767 4.150	2.029 4.952 7.428	58 141 211	68A Nominal (166A) 150% (249A)
6	OTHERI	1.133 2.767 4.150	1.017 2.482 3.722	29 71 106	68A Nominal (166A) 150% (249A)

The A/D is of dual slope integration type and consists of U12B, U2, U11A, U13, U11B, U14, C8, CR14 and some resistors. Chips U11A and U13 together form a counter. Before the start of a conversion cycle, the output of integrator (U12B, C8) is steady at +0.7v; hence the output of comparator U2 is low, and the counter is disabled from counting.

When the START CONV command, which is an 8 μsec long pulse, is generated by the microprocessor, the counter is reset to zero and the Q output of U11B (pin 15) is set high, opening the three gates U14D, U14C, U14B; hence the MUX address (PIA-36, PIA-30, PIA-12) will appear in inverted form at the address input of the multiplexer chip, U17. A current will start flowing in C8 in a direction to ramp the integrator output (U12B-7) negative. The instant this output goes negative, the comparator (U2) will switch high, thus enabling the counter (U11A, U13) to count. When the count reaches 255, pin 13 of U13 will switch from low to high, thus resetting the Q output of U11B which causes the address inputs of the multiplexer to be all high.

The reference voltage (-8.96v) is now selected by the multiplexer, which causes a negative current to flow into the integrator. This current will cause the integrator output to ramp into the positive direction. The counter is now counting up starting from zero. The instant the integrator output goes positive, the comparator will switch low, thus stopping the count. The final count will be proprotional to the analog input. Figure 4-21 shows some of the signals present in the A/D converter.

The ground current sensor, which measures the ground current in the generator, has a voltage output which goes from 0 volts to 5 volts, with 5 volts corresponding to 10 mA of ground current. The sensor outputs are brought to P1A-31 and P1A-32 of the I/O board, as can be seen in Figure 4-20. If the ground current is greater than 5.5 mA (2.75 volts sensor output) a latch on the I/O board which consists of U1B and U1C will latch high, thus making P1B-36 high. The microprocessor will then read this discrete input and decide that there is a ground fault.

RIPPLE MONITOR (P1A-39) is the ac part of the bus voltage. If this exceeds 24 volts p-p, then EXC RIPPLE (P1A-29) will go high, thus indicating a ripple fault to the microprocessor. A peak detector followed by a level detector determines the state of EXC RIPPLE.

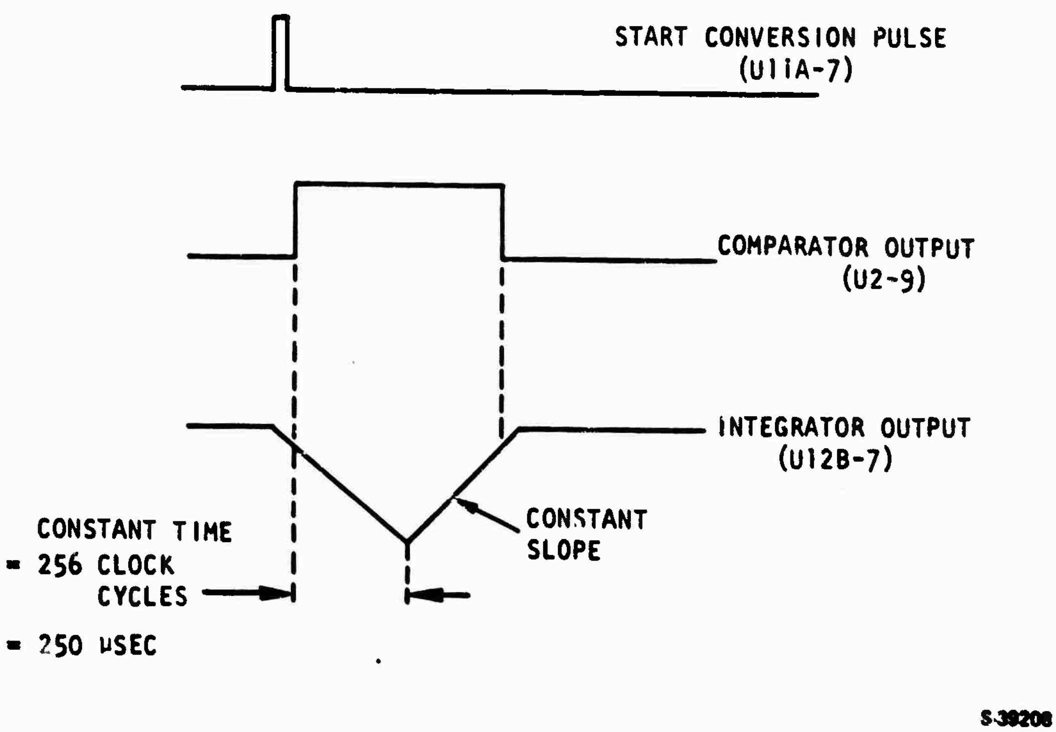


Figure 4-21. A/D Converter Signals

The input marked UNFILTERED AC (P1A-43) is not used in the final configuration. There is no input signal available at that point. In the initial design phases of the generator, the unfiltered output of the phase-delayed rectifier was brought from the generator to the GCU in cable J2, passed through a capacitor in the chassis of the GCU to remove the dc part, and the output of the capacitor was then brought to P1A-43 of the I/O board. FAULTED RECTIFIER (P1B-14) would then go high if UNFILTERED AC (P1A-43) exceeded a certain peak-to-peak value. The microprocessor would then read FAULTED RECTIFIER (P1B-15), and if this logic signal was high the microprocessor would conclude that there was a faulty SCR. This idea was later abandoned because a faulty SCR would show up in excess ripple and would thus be detected by the microprocessor.

ENABLE SCR (P1B-34) and ENABLE GCB (P1B-26) are controlled by the microprocessor. If the OFF/TEST/ON switch is in the OFF position, ENABLE SCR will not go through, and PDR INH (P1B-23) will be low, thus disabling the SCRs. For the ENABLE GCB signal to go through, the OFF/TEST/ON switch must be in the ON position.

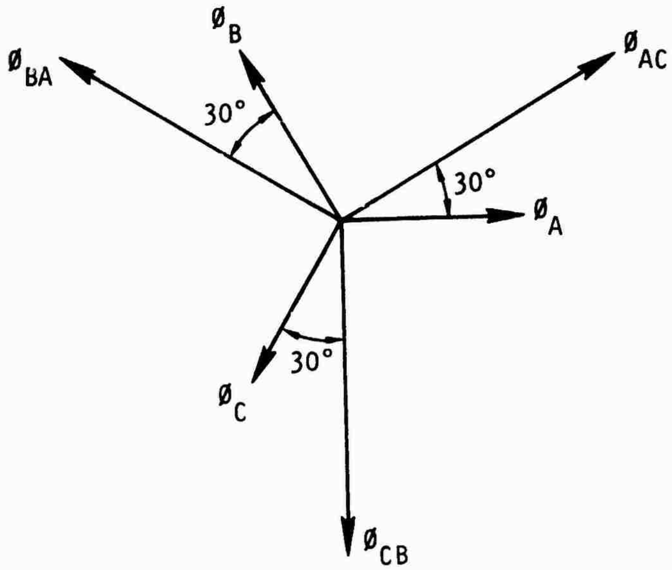
The 5-volt supply goes through a transistor switch whose output is designated as 5V INHIBIT and is available at P1A-5. This signal (5V INHIBIT) goes to PDR boards A1 and A2, where it provides base drive for the transistors which control the firing pulses for the SCRs. If the 5-volt supply is less than 4V, the switch is open, and the SCRs will therefore be disabled. The switch will close when the power supply voltage is above 4V. Comparator U19 controls the state of the switch.

PDR Logic

Boards A1 and A2 in the GCU contain the circuitry which generates the twelve pulses which are necessary to fire the twelve SCRs present in the PDR converter. The generator has two main windings, W1 and W2, with W1 leading W2 by 30 degrees. The six SCRs associated with each winding must be fired 60 degrees apart. Hence, if all twelve SCRs are considered together, there should be twelve firing pulses evenly spaced at 30 degrees apart.

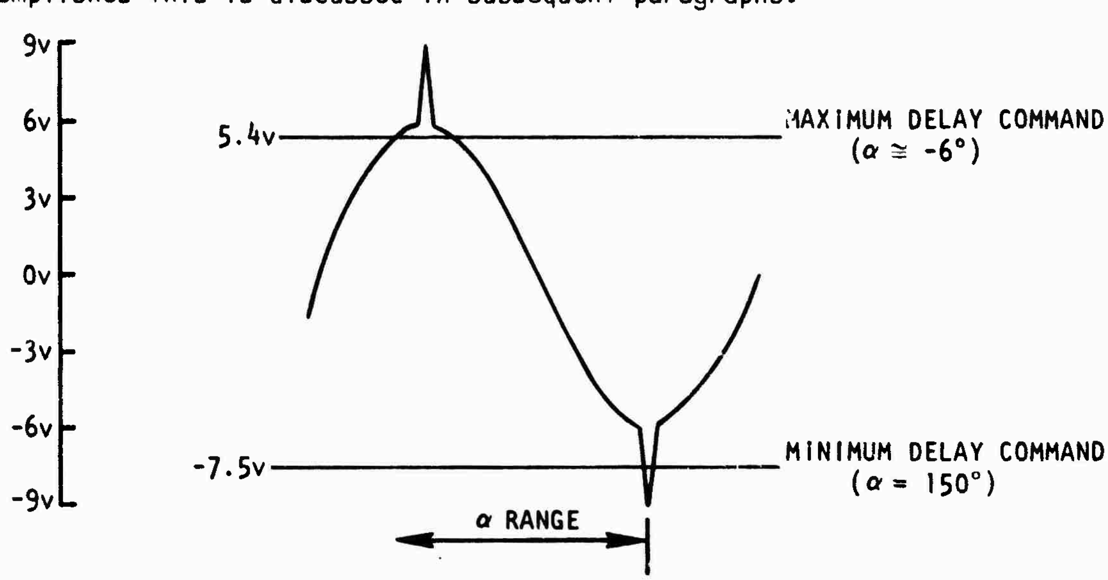
Boards A1 and A2 are identical but not interchangeable. This difference is explained later in this discussion. Drawing 2106404 (Figure 4-22) is the schematic of boards A1 and A2.

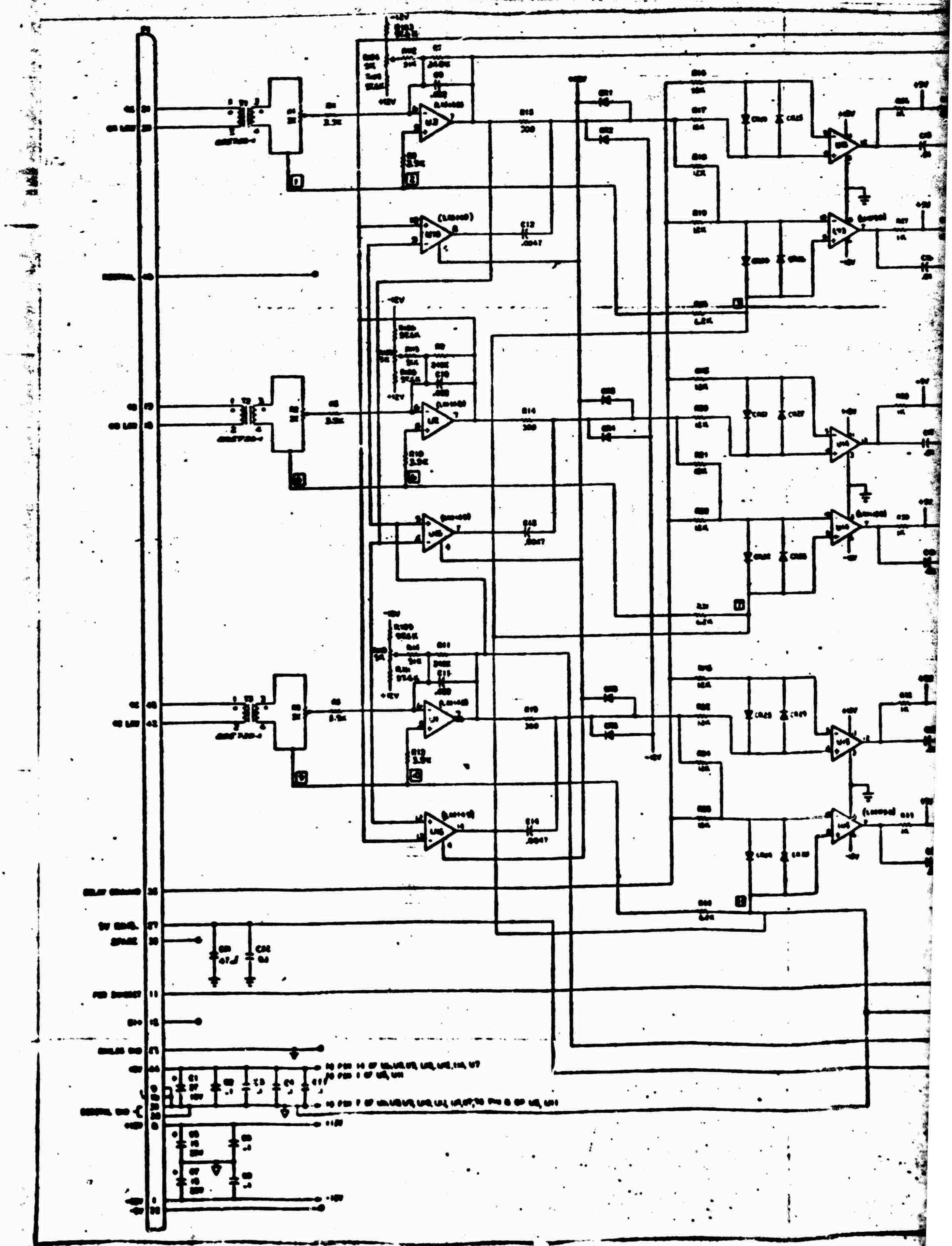
Board A1 generates the firing pulses for the leading winding, W1, whereas board A2 generates the firing pulses for the lagging winding, W2. The generator has an auxiliary winding which is adjusted to be in phase with winding, W1. Board A1 receives its synchronous information from the line-to-neutral voltages of the auxiliary winding, and board A2 receives its synchronous information from the line-to-line voltages of the same winding. Hence board A2 will have its inputs lagging those of A1 by 30 degrees. The following diagram better illustrates the point.

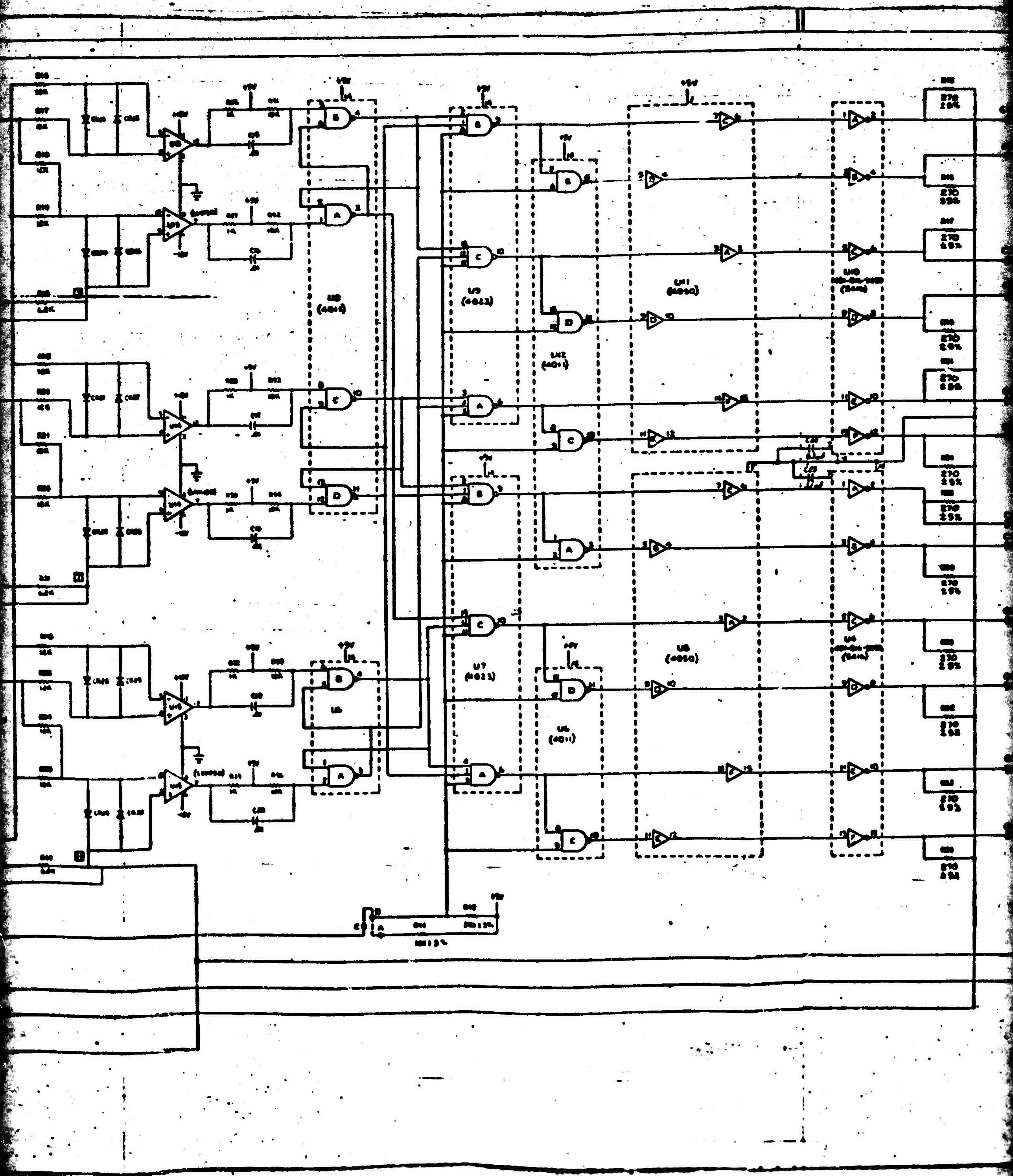


Because of this phase shift, the pulses coming out of board A1 will lead those coming out of A2 by 30 degrees. Figure 4-22 shows that each of the three input phases passes through a transformer (T1, T2, T3), a pot (R1, R2, R3) and is then integrated. The outputs of the integrators (U3-7, U2-7, U1-7) are adjusted to be 12 volts peak to peak. Since board A2 receives line-to-line voltages and since these are larger in magnitude than line-to-neutral voltages, it follows that the settings of pots R1, R2, R3 are different from board A1 to board A2.

Each of the three integrators has also an offset adjustment pot. Figure 4-23 shows the inputs and the outputs of the three integrators. Figure 4-23 also depicts the command (also called delay command) which is a dc voltage generated on board A3, the I/C board (Figure 4-20). The delay command is the output of a 741 operational amplifier and is limited by two zener diodes to 5.4 V (= 4.7 + 0.7) in its positive excursions and to -7.5 V (= 6.8 + 0.7) in its negative excursions. Each integrator output has a 3V blip added to it at its peaks, as shown in the following sketch. The detailed circuitry which accomplishes this is discussed in subsequent paragraphs.







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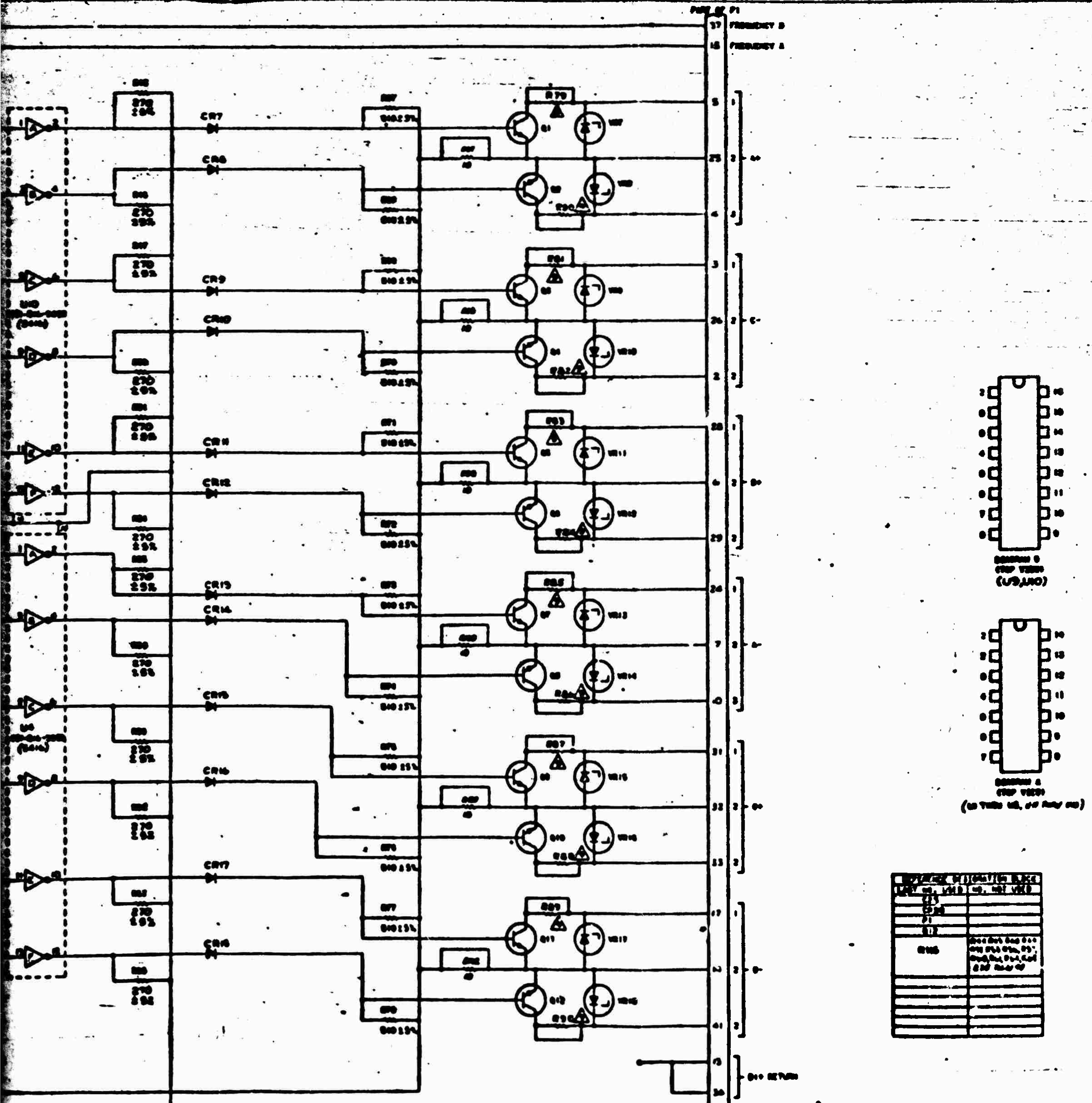
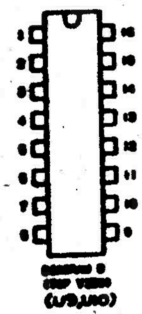


PROVISIONAL COMPONENTS

Sch
PDR
210

12



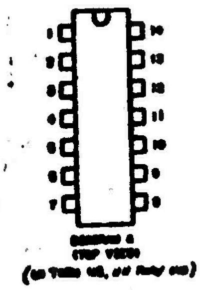


Figure 4-22

Schematic Wiring Diagram,
PDR Logic Boards A1 and A2,
2106404

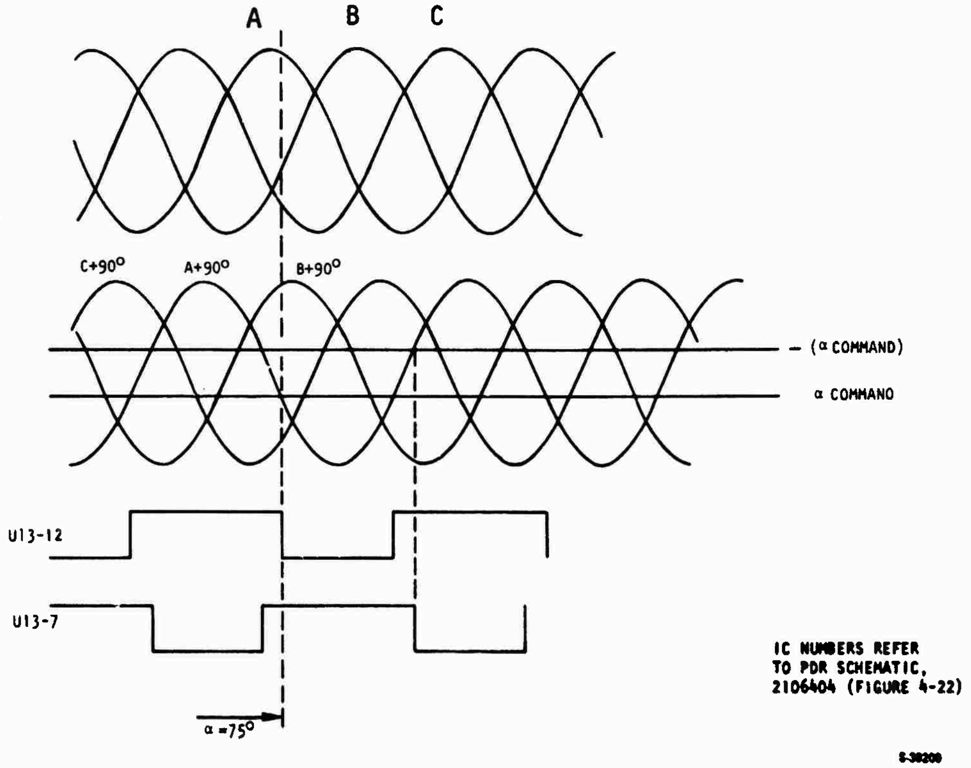


Figure 4-23. Auxiliary Winding Outputs and Integrator Outputs

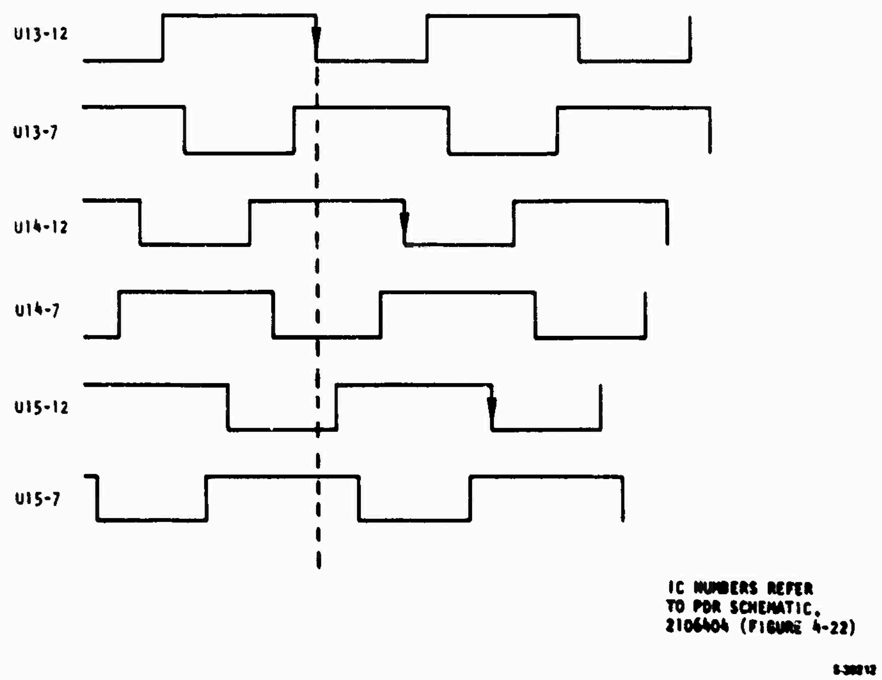


Figure 4-24. Comparator Outputs

Each integrator output is compared to +(α command) and -(α command) with the comparator outputs shown in Figures 4-23 and 4-24. The negative-going edge of U13-12 determines the firing angle α. Waveform U13-7 is obtained by comparing the sine wave with -(α command). The negative-going edge of this waveform lags that of U13-12 by 180 degrees. This is helpful in generating the next set of waveforms shown in Figure 4-25. These have the shape of a square wave.

We now have three square waveforms (U8-4, U8-10, U6-3) corresponding to the three phases and three waveforms (U8-3, U8-11, U6-3) the complement of each of the first three. If we form the six logic products AB', AC', BC', BA', CA', CB', then we get six pulse waveforms as shown in Figure 4-26. These are spaced 60 degrees from each other and have an on-time to off-time ratio of 1 to 2. This ratio results in having a net volt-second of 0 v-sec in the transformers driving the SCR gates.

Chips U11 and U5 provide buffering between CMOS and TTL logic.

The logic signal PDR INHIBIT comes from the I/O board and when high will disable firing of all SCRs. The signal marked 5V INHIBIT provides power to the bases of the output drive transistors. This power input is also coming from the I/O board and will stay at 0 volts until the power supply +5V output reaches 4 volts, whereupon power will be available at this input. For a full description of the circuitry which accomplishes this refer to the Input/Output (I/O) Interface discussion. The above mechanism assures that the SCRs are prevented from being turned on if the GCU power supply is not fully on.

The following is a more detailed description of the integrator and the blip generating circuitry.

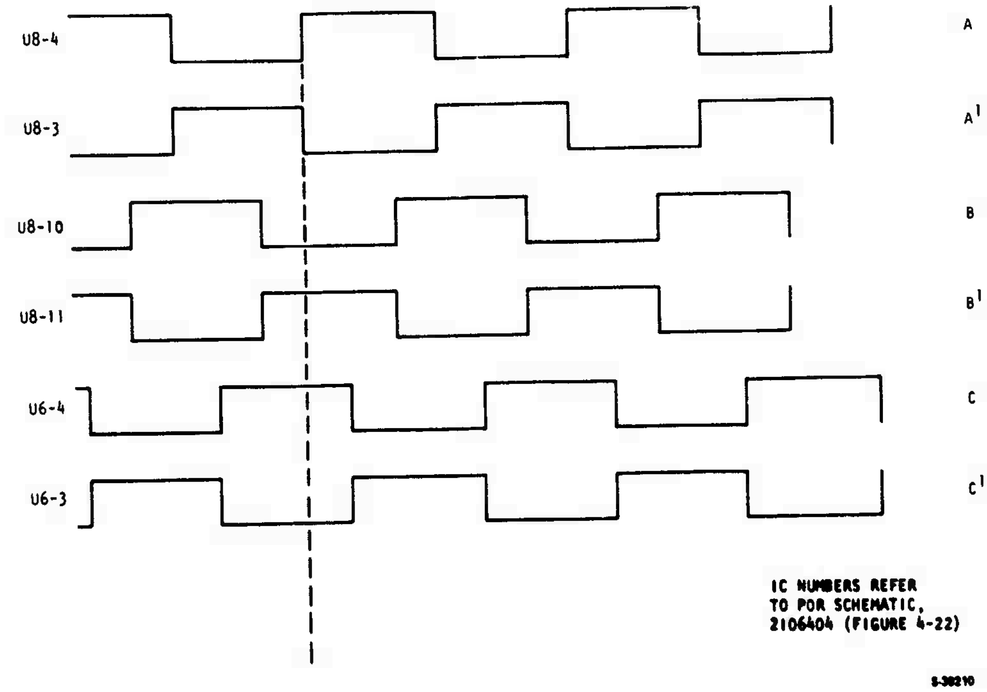


Figure 4-25. Latch Outputs

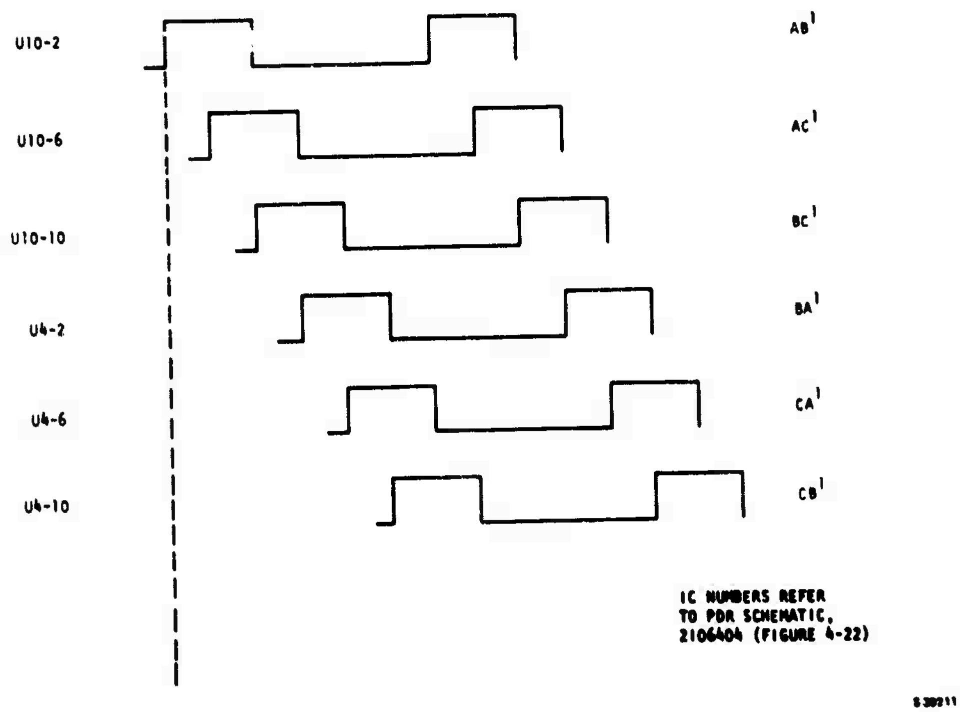
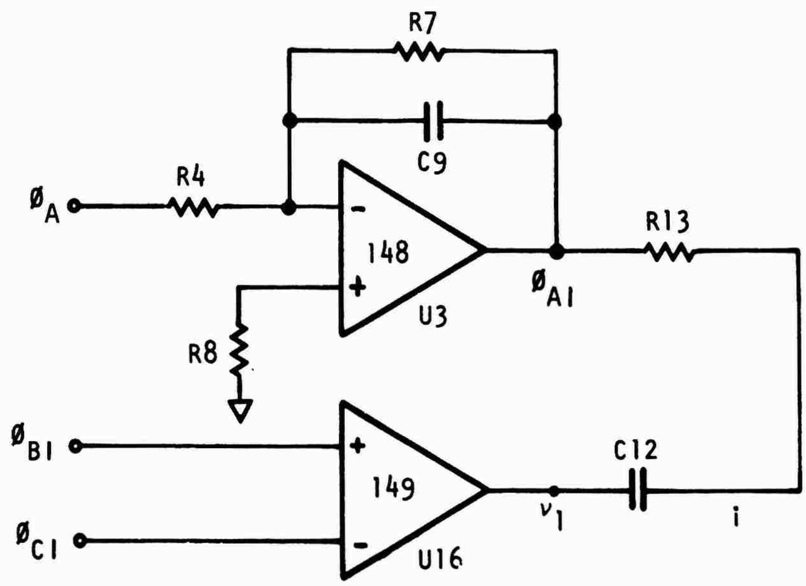


Figure 4-26. SCR Gate Control Signals



$\emptyset_{AI}$, $\emptyset_{BI}$ and $\emptyset_{CI}$ are the integrated outputs of the three integrators. As can be seen from Figure 4-23, $\emptyset_{AI}$ is maximum or minimum when $\emptyset_{BI}$ and $\emptyset_{CI}$ are equal. Hence the output of U16 in the above diagram will switch at the peaks of $\emptyset_{AI}$. The output of LM149 will slew at the rate of 2V/ sec.

$$i = C_{12} \frac{dV_c}{dt}$$

$$\frac{dV_c}{dt} \quad \frac{dv}{dt} = 2V/\mu sec$$

If I = 10 mA, then:

$$C_{12} = \frac{10 \times 10^{-3}}{2 \times 10^6} = 5 \times 10^{-9} f = 5 \text{ nf}$$

$$\boxed{C_{12} = 0.0047 \mu f}$$

If we want a 3V blip, then:

$$i R_{13} = 3V \Rightarrow \boxed{R = 300}$$

Note that, at this point, the blip does not distort the sine wave output of the integrator. The input frequency can be anywhere from 900 Hz to 1800 Hz. The latter corresponds to a period of 555 µsec.

$$R_{13}\ C_{12} = 300 \times 5 \times 10^{-9} = 1500 \times 10^{-9} \text{ sec}$$

$$R_{13}\ C_{12} = 1.5\ \mu\text{sec}$$

Hence there will be no distortion of the sine wave.

To prove that U3 acts as an integrator, we should show that the reactance of C9 is much lower than R7 at the lowest frequency of operation.

$$X_c = \frac{1}{WC_9} = \frac{1}{(2\pi)(900)(.022 \times 10^{-6})} = 8K$$

Hence $X_c << R7$

270VDC GCU Power Supply

Drawing 2106482 (Figure 4-27) is the schematic of the power supply. The 270 vdc power supply generates the following voltages to a ± 5 percent accuracy.

+5V	1 amp
+5V	-1 amp
+12V	0.25 amp
-12V	0.25 amp
+28V	0.45 amp
+270V	0.5 amp
-5V	0.2 amp
-8.96V	0.1 amp

These voltages are generated from an input voltage of 46V to 92V rms, 900 Hz to 1800 Hz. This input voltage is rectified, filtered and preregulated to 70 vdc, which is then fed to an inverter which generates the above voltages.

This dc power supply consists of four basic sections:

- Logic and control
- Switching regulator
- Inverter
- Output rectifiers and filters

The logic section utilizes a pulsewidth modulator (PWM) integrated circuit U3. This circuit performs the functions of oscillator, ramp generator, flip-flop, and gating. The output of the PWM IC is buffered by compartor U1, which drives transistors Q5 and Q6. These transistors drive the primary of transformer T_1, which is used to provide isolated base drive to the switching regulator transistors Q5 and Q6 (chassis) and the inverter transistors Q1, Q2, Q3, Q4 (chassis). Transistors Q1, Q2, Q3, Q4 and VR1 through VR3 form a series pass regulator which provides power to the logic circuitry and the primary of transformer T_1 during the power supply start-up sequence.

Also included in the control section are the comparator U_{2D}, which enables the power supply when the line voltage is adequate for regulation, and the operational amplifier U2, which is the control error amplifier. This amplifier compares the power supply reference voltage, which is generated by the PWM IC, to an isolated feedback voltage. The resultant error voltage is used by the PWM IC to generate the duty cycle of the power supply. A noteworthy feature of the PWM IC is a deadtime adjustment composed of R_{19} and R_{20} which sets the maximum duty cycle allowed for the power supply. This assures adequate off time in the switching regulator transistors Q5 and Q6 (chassis) during the start sequence.

The logic and control section provides the appropriate duty cycle to ensure that the switching regulator output is a waveform whose amplitude and on time product is constant over each cycle. This waveform is then filtered by the components L2 and C3 (chassis) to produce 70 volts dc.

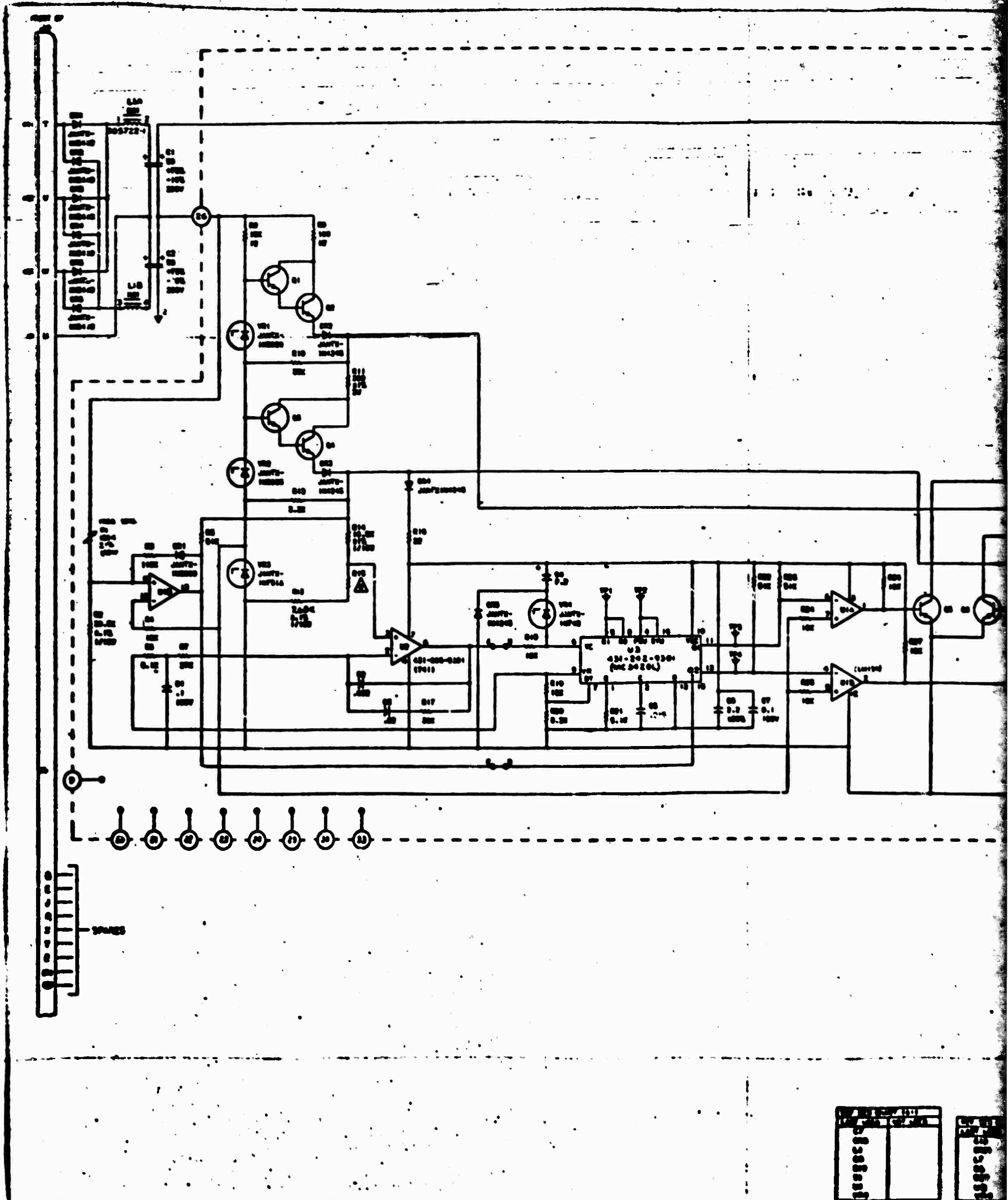
This voltage is utilized as the supply to the inverter and also to back bias the series regulator which powers the primary of T_1 (PM 2). Thus the base drives for the switching regulator and inverter transistors are derived from a regulated voltage source immediately after power supply start-up, thereby enabling the power supply efficiency to be independent of the input line voltage.

The output voltage of the switching regulator is utilized by the inverter to generate the output voltages. The inverter is driven by the switching regulator control circuitry. Feedback windings (15, 16, 17 and 18) on transformer T_1 (chassis) assure a square wave at the output of the inverter. As a result, minimal filtering is required at the output in order to generate the dc voltages.

Loop Dynamics

Since the loop gain of the generator is proportional to the speed of the generator (output voltage is proportional to speed) the loop was analyzed and compensated at its highest gain or least stable point. The gain of a conventional phase-controlled rectifier is

$$E_o = \frac{3\sqrt{3}}{\pi} V_{\ell-n} \cos\alpha$$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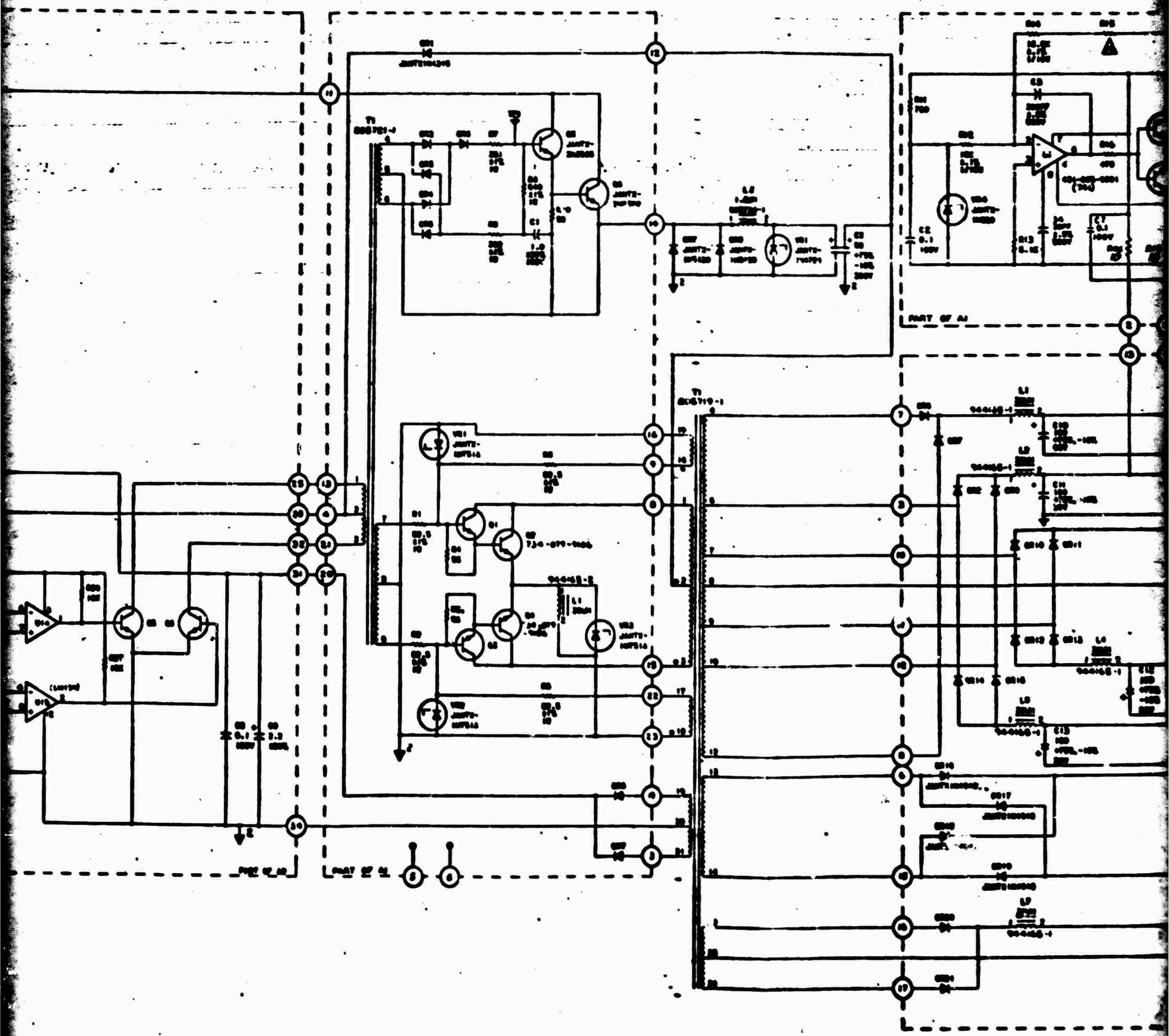

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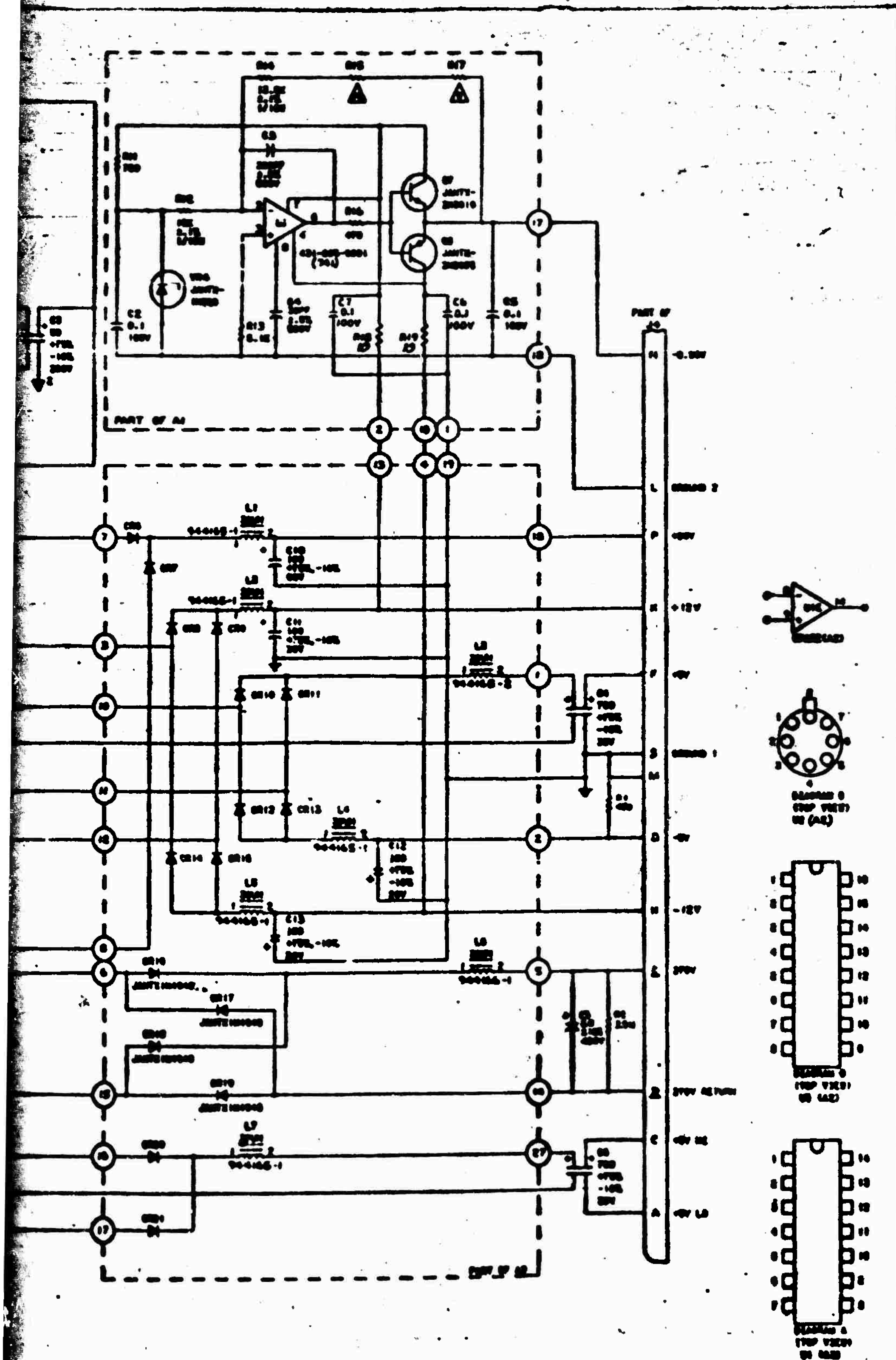


Figure 4-27

Schematic Wiring Diagram, 270 VDC GCU Power Supply, 2106482

3

Figure 4-28 shows the relationships between the commutated voltage, $Va_{\ell-n}$, and the reference used to generate the delay command α. As shown in the diagram, the line-to-neutral voltage $Va_{\ell-n}$ is turned on when $V_{delay\ command} = V_{ref}$ and remains on for 120 degrees, at which point the next phase is turned on. Since

$$V_{delay\ command} = V_{ref} \cos \alpha$$

$$\alpha = \cos^{-1} \frac{V_{delay\ command}}{V_{ref}}$$

$$\therefore E_o = \frac{3\sqrt{3}}{\pi} V_{\ell-n} \frac{V_{delay\ command}}{V_{ref}}$$

or

$$G_1 = \frac{V_o}{V_{delay\ command}} = \frac{3\sqrt{3}}{\pi} \frac{V_{\ell-n}}{V_{ref}}$$

$$V_{\ell-n} = 365v \times \sqrt{2} = 569$$

$$V_{ref} = 6v$$

$$G_1 = 157 \frac{v}{v}$$

$$\frac{V_{in} \dfrac{R_2}{R_1 + R_2}}{R_3 + \dfrac{R_1 R_2}{R_1 + R_2}} = i_o$$

$$\frac{V_{in}}{i_o} = \frac{R_3 + \dfrac{R_1 R_2}{R_1 + R_2}}{\dfrac{R_2}{R_1 + R_2}}$$

$$= R_3 \frac{R_1 + R_2}{R_2} + R_1$$

$$= R_3 \left(1 + \frac{R_1}{R_2}\right) + R_1$$

$$= 4.421\ M\Omega$$

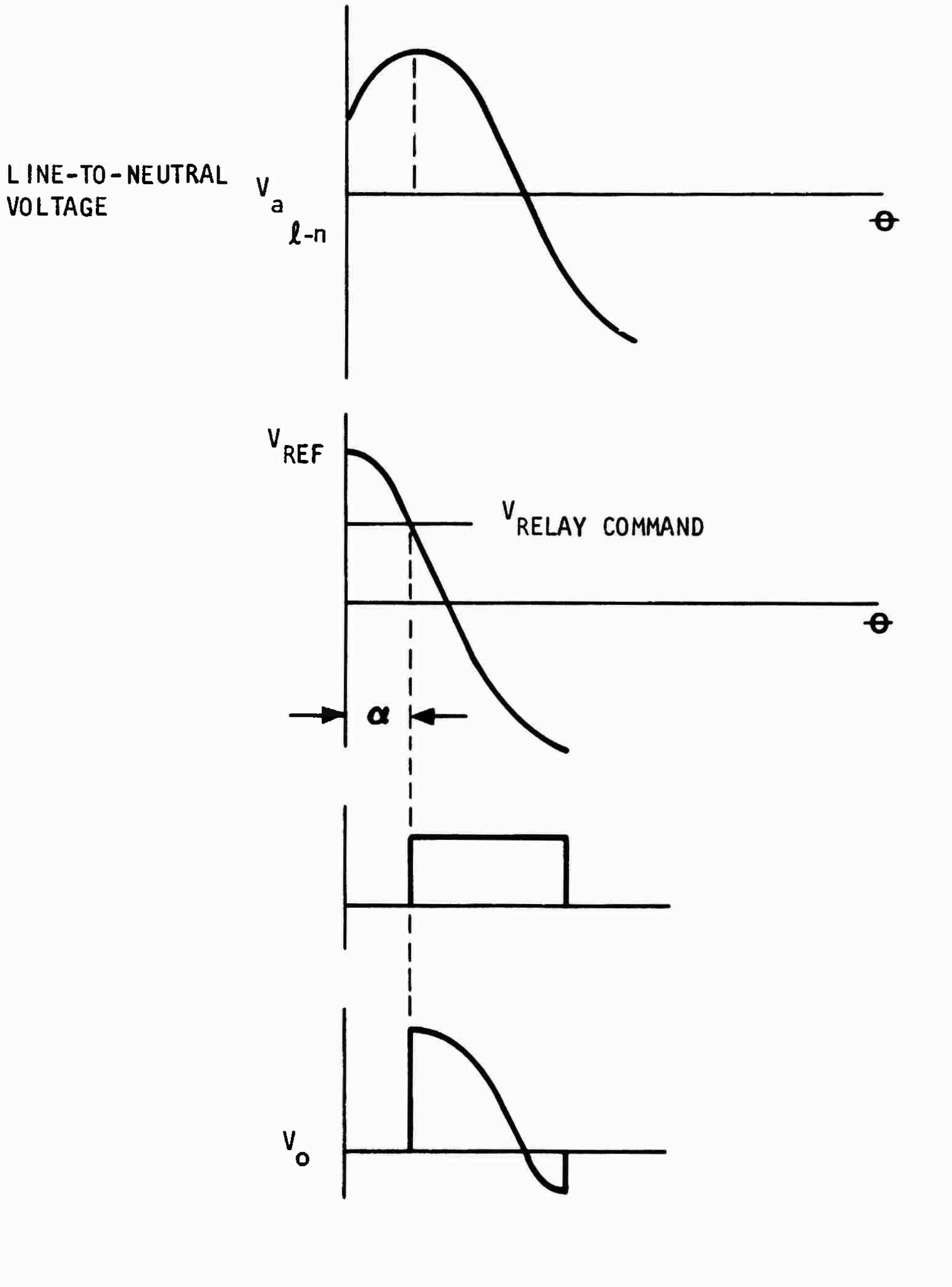


Figure 4-28. Loop Dynamics Time Relationships

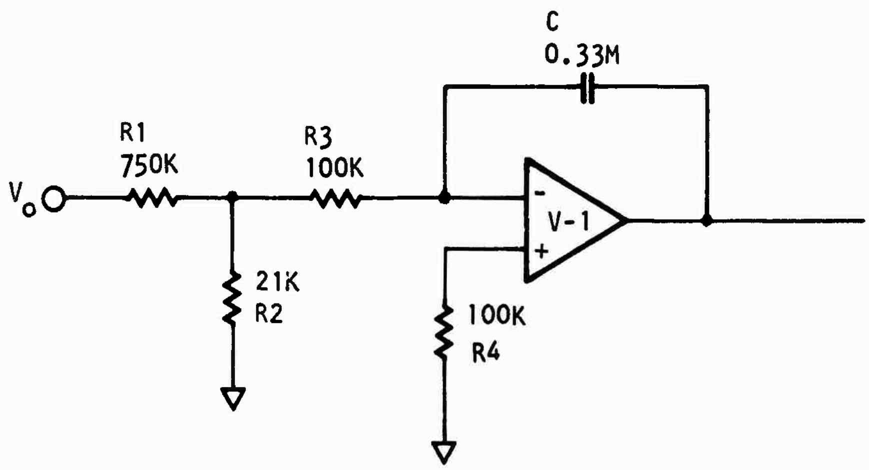
$$G = \frac{1}{RCS} = \frac{1}{4.421M \times .33\ \mu s} = \frac{1}{1.459} \cdot \frac{1}{s}$$

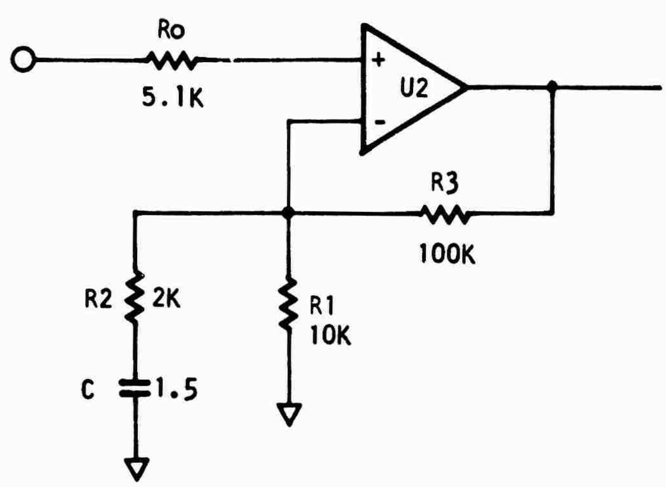
$$= 0.685 \cdot \frac{1}{s}$$

$$G = \frac{R_1 + R_3}{R_1} \cdot \frac{\left\{\left(\frac{R_1}{R_1 + R_3} R_2 + \frac{R_3}{R_1 + R_3} (R_1 + R_2)\right) CS + 1\right\}}{R_2CS + 1}$$

$$G = \frac{\left(\frac{S}{60.1} + 1\right)}{\left(\frac{S}{333} + 1\right)}$$

The remaining elements in the loop and the derivation of its transfer functions are shown in the following sketches.





The last element in the loop is the filter on its output which consists of the machine's leakage inductance of 85 μh and the inductance of its interphase transformer, 65 μh, and the output filter capacitor, 12 μf.

The block diagram of the loop is shown in Figure 4-29. Loop gain is shown in Figure 4-30.

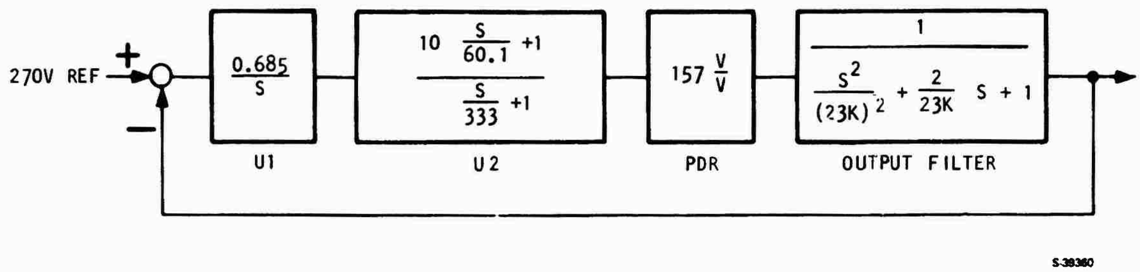


Figure 4-29. Block Diagram, Transient Voltage Regulation Loop

ROTATING MACHINE

The electromagnetic design of the generator was optimized early in the program by using the AiResearch permanent-magnet machine performance prediction computer program. The design attempted to achieve the lightest weight generator compatible with the phase-delay rectifiers and consistent with system objectives (such as good efficiency and voltage regulation), and thermal and structural design considerations. Magnet size and shape was also optimized to satisfy stress requirements. The effect of the following variables was investigated:

- Number of poles
- Stator lamination material
- Permanent magnet configuration
- Machine length-to-diameter ratio
- Commutating reactance
- Air gap length.

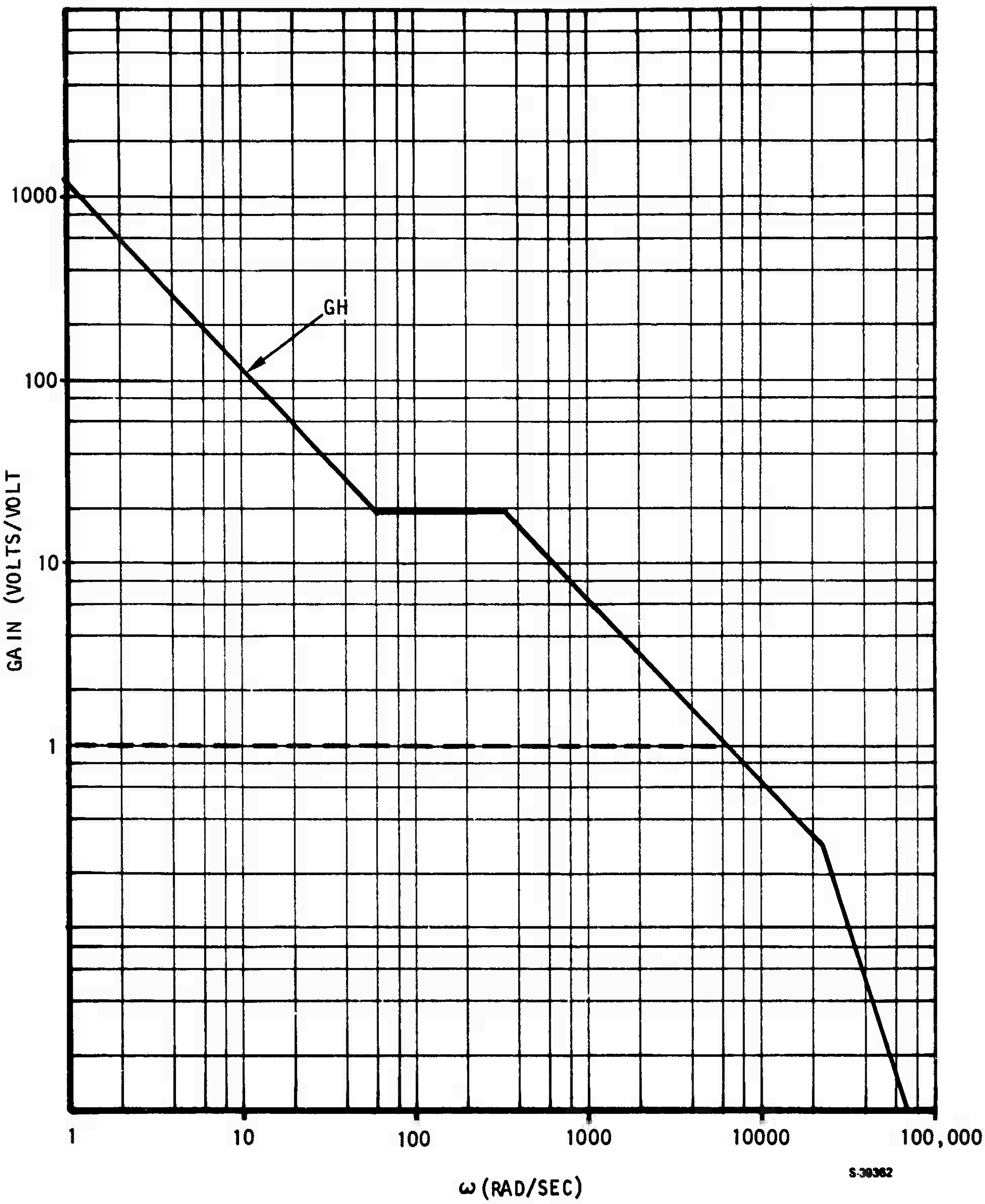


Figure 4-30. Loop Gain

The significance of these parameters and the reasons for the final selected configuration are discussed below.

NUMBER OF POLES

The selected 12-pole configuration is advantageous for several reasons:

(a) Optimum flux focusing is obtained as compared to a small number of poles.

(b) Ripple frequency of a 12-pole machine is high, so the filter size is small.

(c) Stator end coil extension and stator core height and weight are small.

A larger number of poles was not desirable for these reasons:

(a) Stator slots become too small for this bore diameter and a good fill factor for the winding cannot be achieved. Using a large diameter to achieve a larger slot increases rotor stress and also results in a shorter stack length. With a shorter stack length, end-leakage effects in magnets and stator coils are relatively higher and result in a nonoptimum magnet design.

(b) Iron losses at the high-speed end are more dominant.

(c) Rectifier circuit losses and cooling present greater problems as the number of commutations per second increases.

STATOR LAMINATION MATERIAL

Vanadium Permendur lamination material versus high silicon steel was investigated. Although the Permendur has higher saturation capability, 0.007-inch thick silicon steel material was selected to obtain lower losses for the operating frequency range. This facilitated cooling the machine, improved efficiency, and has a significant cost advantage.

PERMANENT MAGNET CONFIGURATION

The geometry of the magnet was manipulated within the constraints of the 12-pole tangential orientation rotor structure. This was necessary in order to optimize the rotor design for best magnetic, stress, and thermal performance.

MACHINE LENGTH TO DIAMETER RATIO

The aspect ratio of rotor diameter to length was varied to obtain acceptable rotor stresses, good electromagnetic characteristics, and acceptable dynamic characteristics.

COMMUTATING REACTANCE

Although the weight of the electrical machine can be reduced by increasing the electric loading and reducing the flux, higher commutation reactance results, and larger filters and higher voltage electronic components are required in the system. Therefore the most propitious reactance from the standpoint of the overall system had to be determined.

AIR GAP LENGTH

The radial magnetic air gap between the rotor poles and the stator teeth is made up of the 0.025-inch thick Inconel 718 sleeve, the 0.025-inch mechanical running clearance, and the 0.030-inch thick carbon filament-wound bore seal. The air-gap value was selected for acceptable values of mechanical running clearance, pole face losses, flux leakage, and bore seal mechanical strength.

Generator design is summarized in Table 4-12.

PITOT PUMP DESIGN

The pump was sized to meet the following design conditions:

	Condition A	Condition B
Cooling fluid	Coolanol 25	Coolanol 25
Fluid temp at generator inlet, °F	250	250
Fluid temp at pump inlet, °F	285 (max)	285 (max)
Flow rate, gpm	1.75	3.50
Pressure rise, psi	41	113
Rotational speed, rpm	9,000	18,000

TABLE 4-12. PERMANENT-MAGNET GENERATOR (CALCULATED DATA)

Rating:

45 kw (continuous), 56.25 kw (2 min)

146 v, L-N, dual 3-phase windings displaced 30 degrees

12 poles

9,000 to 18,000 rpm

Dimensions, inches	Proposed Design	Final Design
Stack OD	5.764	5.825
Bore	4.560	4.56
Slot height	0.397	0.400
Tooth width	0.0915	0.0915
Stack length	3.996	4.086
Stator coil extension	0.74	0.741
Bore seal thickness	0.04	0.030
Rotor OD	4.460	4.440
Rotor poles ID	2.378	2.62
Shaft Id	1.6	1.6
Rotor length	4.396	4.82
Pole width	0.774	0.836
Magnet section	1.012 x 4.396	0.892 x 4.75
Magnet length	0.389	0.350
Effective magnetic gap	0.0701	0.080

Performance and Loss Summary:	At 9,000 rpm		At 18,000 rpm	
	Proposed	Final	Proposed	Final
Load, per unit	1.0	1.0	1.0	1.0
Amp/sq in.	16,153	15,916	15.656	15,916
Amp conductors/in.	1,219	1,161	1,185	1,161
Flux Density, k/sq in.				
Stator core	105.4	104.4	104.3	104.2
Teeth	110.4	116.1	112.2	115.8
Gap	50.7	50.2	48.5	50.0
Pole	92.4	83.2	93.5	83.0
Magnet	26.8	32.4	34.	32.36
MMF, amp-turns/pole				
Armature reaction	-370.6	-323.8	-359.4	-329.8
Core	-30.6	-27.3	-26.5	-26.3
Teeth	-75.	-117.9	-89.4	-115.6

TABLE 4-12 (Continued)

MMF, amp-turns/pole (Cont'd)	Proposed Design	Final Design	Proposed Design	Final Design
Gap	-1112.	-1101.9	-769.4	-1099.0
Pole	-121.8	-118.4	-108.0	-117.5
Magnet	1710.	1689.3	1352.7	1684.2
Flux, k/pole				
Total	238.6	260.2	234.5	259.5
Leakage	-66.2	-62.4	-57.0	-62.2
Net	172.4	197.8	177.5	197.3

Electrical losses, kw	At 9,000 rpm		At 18,000 rpm	
	Proposed Design	Final Design	Proposed Design	Final Design
Stator copper	2.091	1.82	2.091	1.82
Stray	0.0551	0.06	0.110	0.12
Pole head	0.0241	0.06	0.0713	0.18
Teeth	0.374	0.42	0.881	0.99
Core	0.471	0.52	1.109	1.08
Total	3.015	2.88	4.262	4.19
Efficiency, percent:				
Electromagnetic	93.72	94.0	91.35	91.5

Weight Summary, pounds*	Proposed Design	Final Design
Stator:		
Core	3.711	4.346
Teeth	2.948	2.898
Copper	2.193	2.213
Rotor:		
Poles and Dampers	3.797	6.476**
Magnets	6.123	6.87
Total Electromagnetic Parts	18.77	22.833

*See Figure 4-31.
**Lightening holes omitted

TABLE 4-12 (Continued)

Other Data

	Proposed Design	New Design
Stabilized short circuit current, A/Ø (unregulated)	196	188.31
Stator resistance (at 400°F), ohms/phase	0.0825	0.097
Stator winding leakage inductance, mh	0.0537	0.0604

(The stator winding leakage inductance controls overlap angle in the phase-controlled rectifiers. The value is such that a proper electrical interface is maintained between the alternator and the power conditioner.)

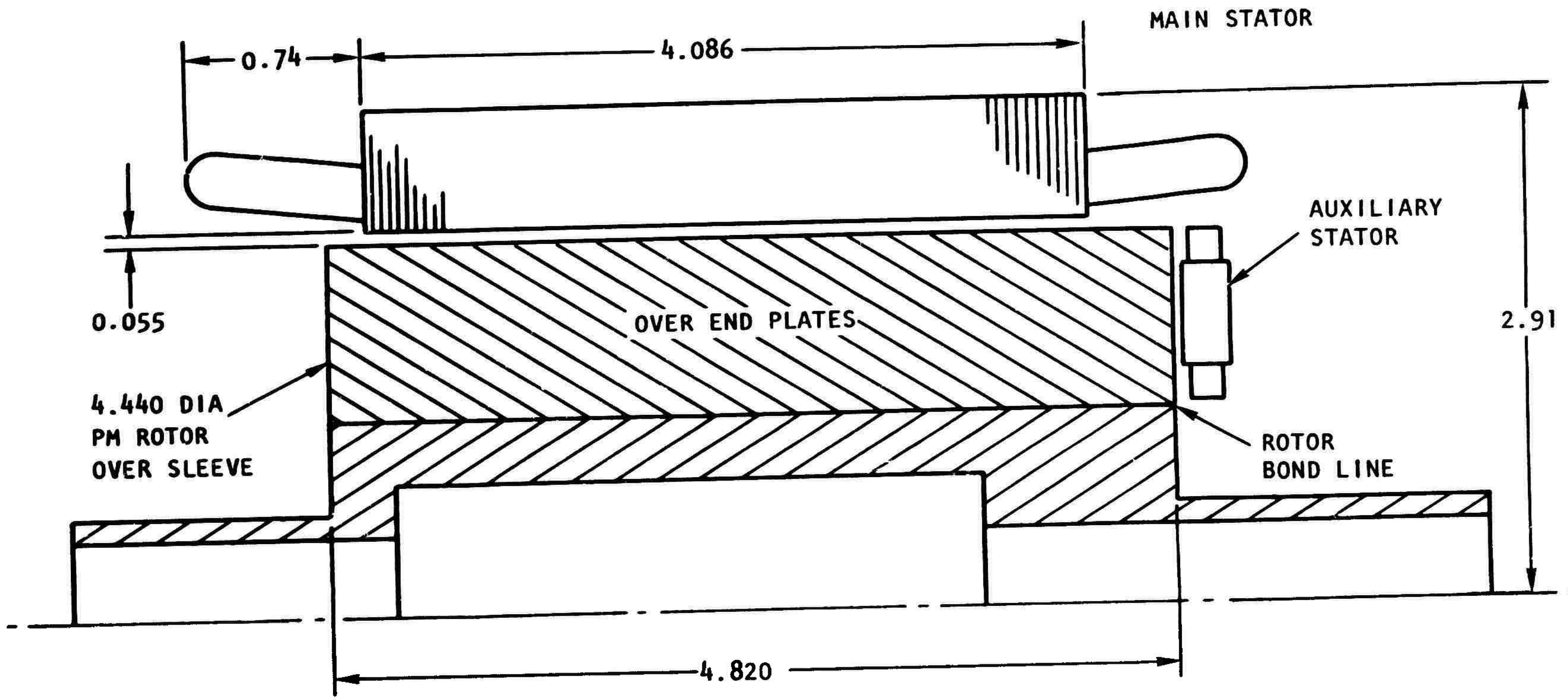
Winding Description (Main Winding):

1. Dual windings, both windings identical except second winding displaced 1 slot (30 elec. deg). No common connections.
2. Each winding composed of 36 coils, wye-connected, 1 circuit, 3 phase.
3. Coil data: Two turns per coil of 34 strands of AWG No. 28 HML, throw 1-6.

Materials

Stator iron	0.007-in. high silicon steel
Conductors	Annealed copper, HML insulated
Rotor poles	Republic HP 9-4-20
Rotor hub	Inconel 718
Magnets	Recoma 22
Insulation	Class 220°C
Bore seal	Filament-wound carbon-resin

Note: Auxiliary Generator winding details are shown in Figure 4-32.

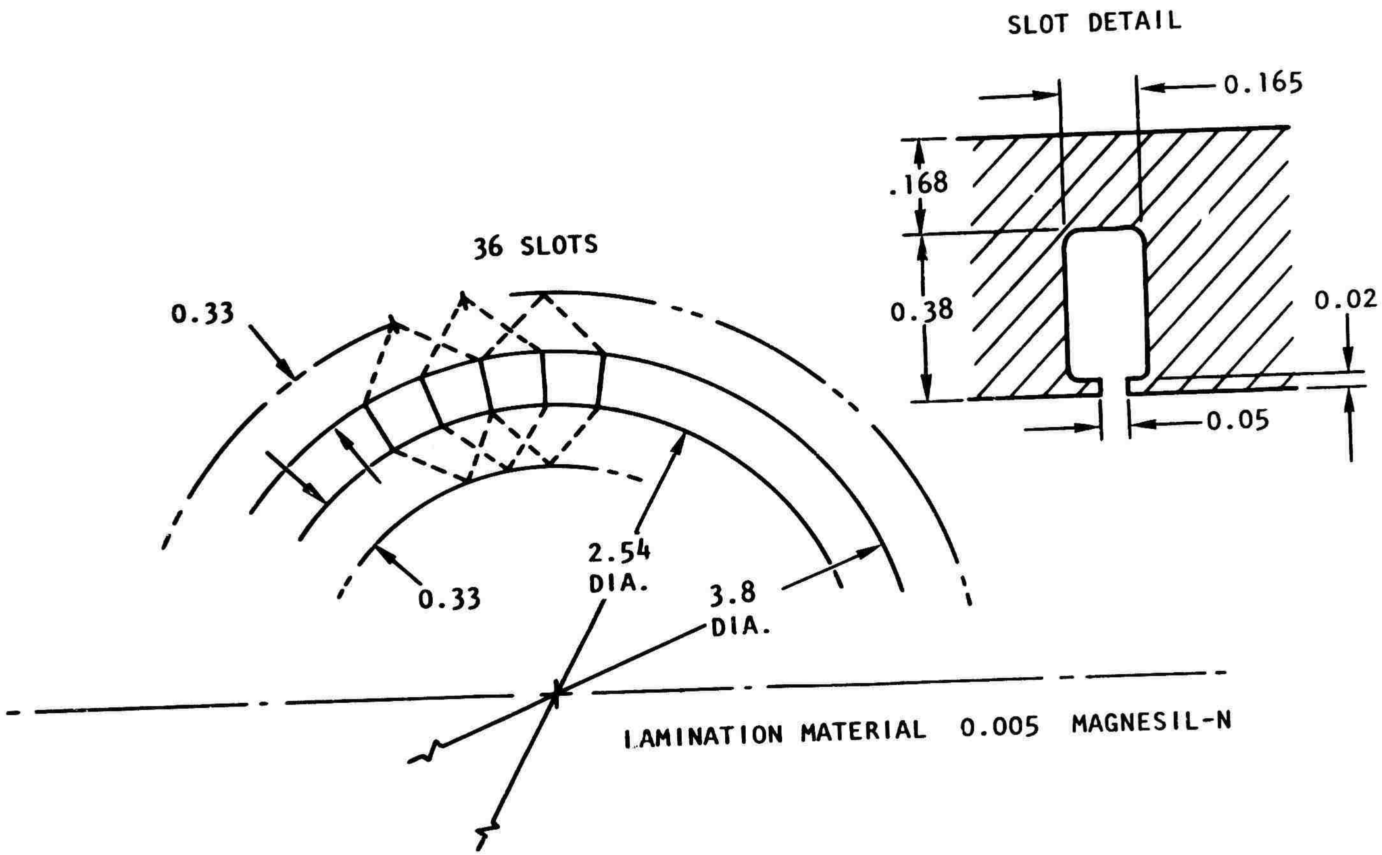


WEIGHT SUMMARY (ELECTROMAGNETIC)

STATOR		ROTOR		AUXILIARY STATOR	0.96
COPPER	3.20	MAGNETS	6.87		
IRON	7.35	POLE IRON	5.78		
		HOOP	0.40		
		END PLATE	0.38		
		SHAFT	4.70		
TOTALS	10.55 LB		18.13 LB		0.96 LB

S-37617

Figure 4-31. Generator Electromagnetic Outline - Final Design



TWO WINDINGS:

FIRST WINDING 8 TURNS, AWG #21
SECOND WINDING 2 TURNS, AWG #20, TWO IN PARALLEL
1-3 THROW, 3 PHASE WYE

1ST WINDING 41V $_{L-N}$, 2.26A, 278 VA

2ND WINDING 10.26/20.52 V_{L-N}, 4.57/6.49, 150/200 VA

S 37618

Figure 4-32. Auxiliary Generator Details

Condition A was used to size the pump, assuming that the rotating impeller is completely filled with liquid. The pump impeller will be only partially filled with liquid while operating at condition B and at most other operating conditions.

The pump is a single-probe pitot pump (Figure 3-10) consisting of a stationary pickup probe located inside a rotating impeller. The flow enters the two-piece pump impeller and flows radially outward through eight passages and then enters the inner chamber through eight holes in the chamber wall. The inner chamber contains eight radial blades on each side of the impeller. The hollow stationary probe receives the flow, diffuses it internally, and delivers it to an annulus near the axis of rotation.

The design of the probe is shown in drawing 2046658 (Figure 4-33). Selected pump geometry is summarized below:

Mean radius of probe inlet area, inches	1.20
Probe inlet area, square inch	0.01188
Impeller internal diameter, inches	2.74
Number of impeller blades	8

The hollow strut portion of the probe is a modified NACA 0018 airfoil with a chord of 0.75 inch, a maximum thickness of 0.135 inch and a trailing edge radius of 0.16 inch. The interior flow passage inside the strut has a cross-sectional area of 0.0238 square inch.

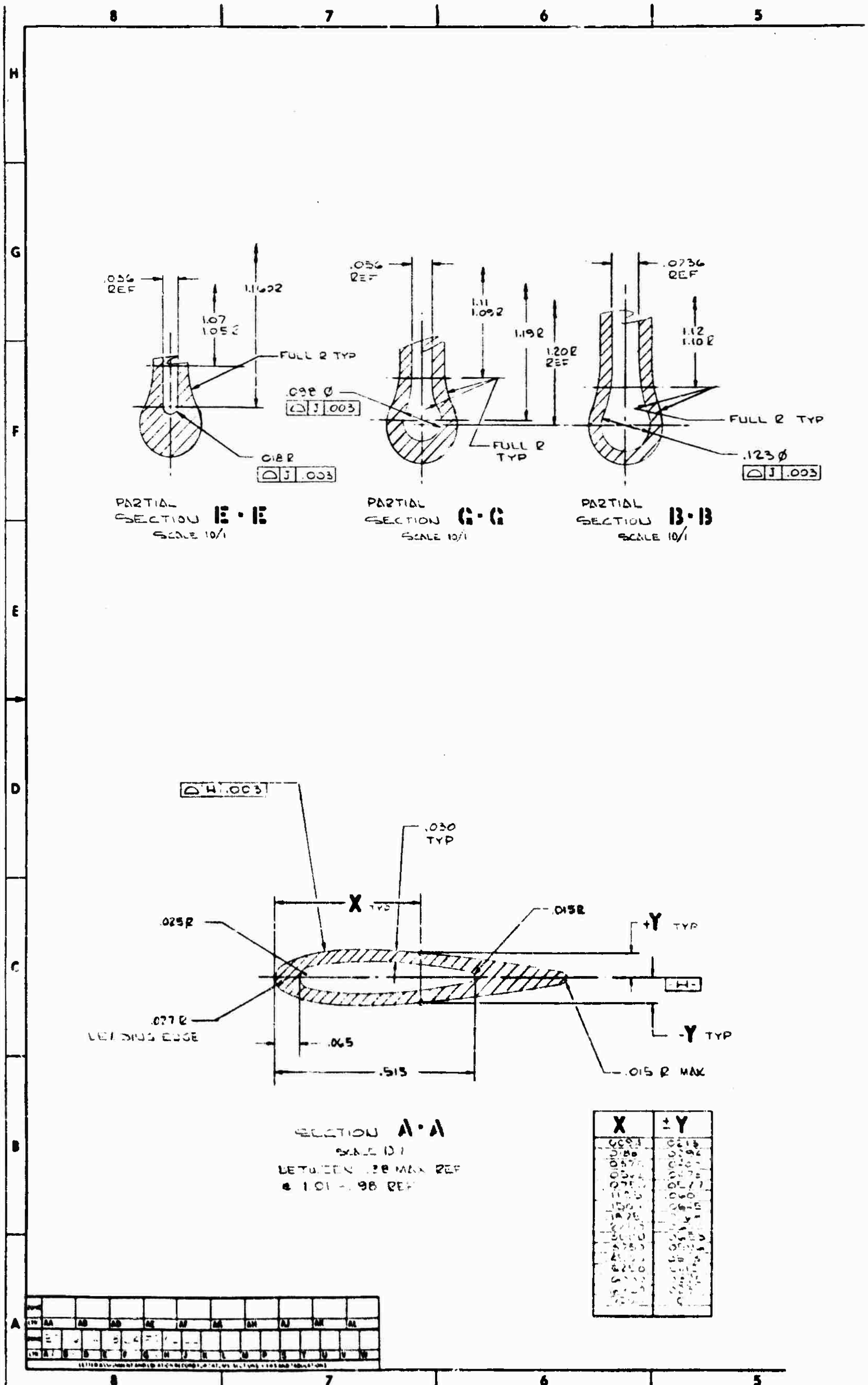
Separate pump development tests were conducted to finalize design clearances and impeller configurations.

PACKAGING

GENERATOR

During initial design and layout of the generator assembly, several problems were encountered with packaging all the power electronics related circuit boards within the main generator housing. Due to insufficient space, thermal considerations, and maintainability requirements, the logic portion of the thyristor gate drive electronics was moved to the generator control unit. This increased the complexity of the GCU and the interconnecting harness.

The gate drive transformer circuit board was packaged in close proximity to the thyristors to minimize lead inductance and noise pickup. The cable assembly from the generator connector to the circuit board was shielded to provide additional EMI and mechanical protection, and all control wires were twisted to minimize inductance. The individual interconnecting wires were secured with wire clamps and tie cords, and additional nomex-rapton-nomex insulation was provided in critical, close proximity, and vibration-prone areas.



S-38518

Figure 4-33. Pitot Pump Probe Assembly, 2046658 (Sheet 1)

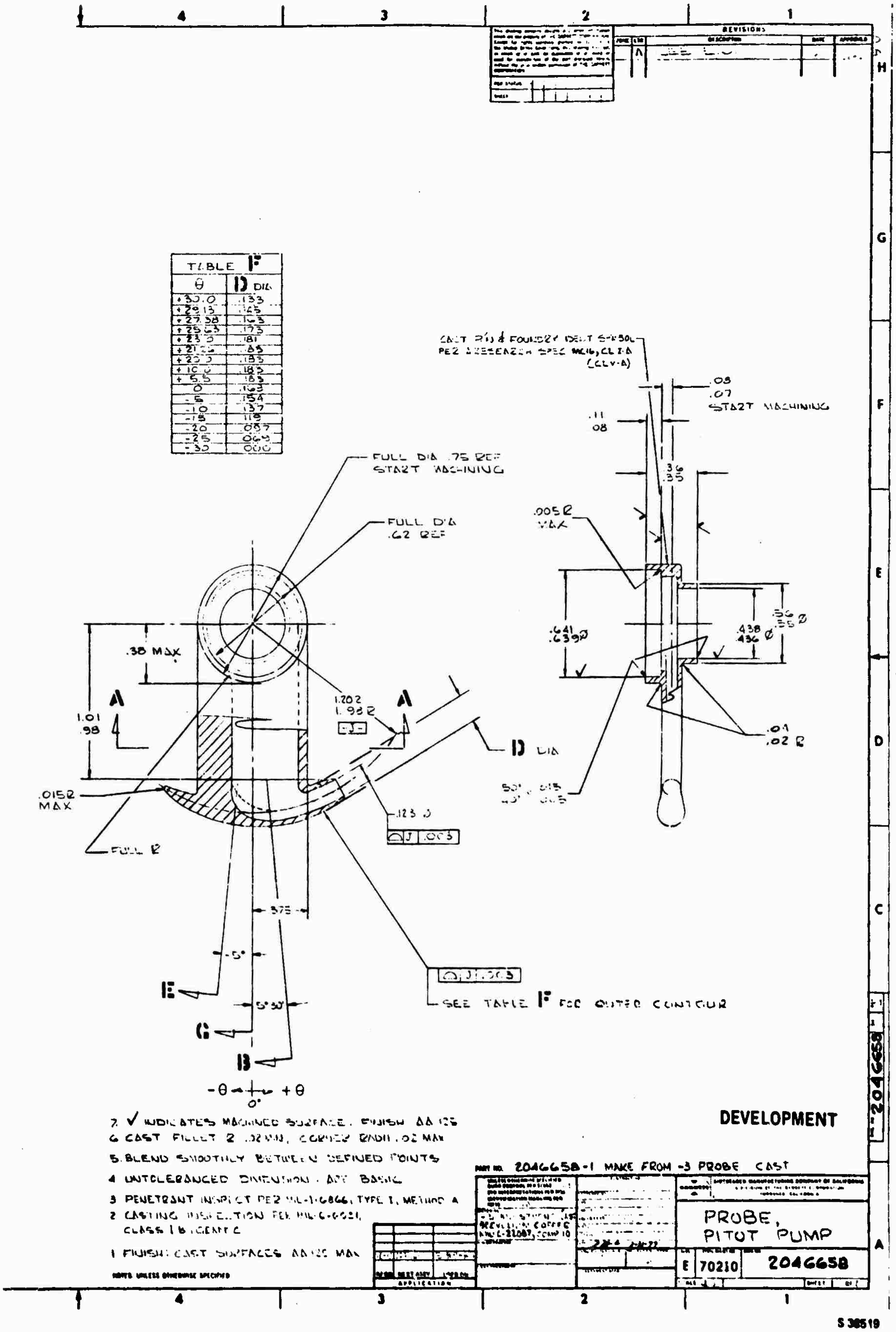


Figure 4-33. Pitot Pump Probe Assembly, 2046658 (Sheet 2)

Final packaging and coolant loop interconnection of the interphase transformer and ripple inductor necessitated "doghouse" and slight "bump" modifications of the generator cover assemblies.

GENERATOR CONTROL UNIT (GCU)

The GCU package is a modularized package consisting of four PC boards, a power supply, and an EMI filter assembly. During the layout phase several iterations of the package were made in order to accommodate increased circuitry from the generator housing while keeping the size and weight within acceptable limits. The final design has the following features:

- Modular construction
- Power supply isolated for EMI
- Plug-in modules
- Wire-wrap interconnect
- Microprocessor isolated

During the system development an arc-over occurred between adjacent pins of the wire-wrap connector. This arc-over was the result of bringing the 270V sense point into the unit. The system wiring was changed to ratio the sense voltage down at the point of regulation, thus ensuring that no high voltage was brought to the unit.

The unit was designed and fabricated to AiResearch standard drawings and manufacturing procedures, which are compatible with typical military requirements. The GCUs were classified as research hardware in order to expedite development changes through the Manufacturing, Procurement, and Design groups.

SECTION 5

PERFORMANCE VERIFICATION

COMPONENT AND SUBSYSTEM DEVELOPMENT AND TESTING

Critical system components and subsystems were separately evaluated and developed to assure maximum confidence level during system integration.

COMPONENT TESTING

Rotor Magnets

To assure generator performance, each magnet was tested at the manufacturer's facility. A typical magnet curve is shown in Figure 5-1. It can be seen that the required 22 MGD energy product was achieved. The magnets were also visually inspected for mechanical integrity and dimensional conformance.

Rotor Assembly

Due to the nature of the wedged 12-pole type rotor assembly, bimetallic joint development was undertaken to assure high strength bond between the magnetic pole section and the nonmagnetic hub. After several unsuccesful brazing cycles, the rotors were hot isostatic pressure (HIP) bonded and heat treated. Joint integrity was proved by spinning the rotors to 33,800 rpm for one minute without the magnets, as shown in Figure 5-2. The flywheel at the rotor end was added to stabilize the rotating part without the magnets. After dimensional and Xyglow inspection, the magnets were installed and the assembly was processed as follows:

(a) Inspect and record OD of rotor.

(b) Soak rotor at 350 $\pm 25°F$ for one hour before mounting in overspeed fixture.

(c) Overspeed rotor to 19,000 rpm for one minute, reduce to 0 rpm; repeat four times.

(d) Apply resilient, high-temperature potting compound behind magnets.

(e) Finish machine, install Inconel 718 end plates and sleeve; finish grind outer diameter.

(f) Final balance and repeat steps a, b, and c.

Figure 5-3 shows the rotor-magnet assembly before installation in the spin pit.

A typical data sheet is shown in Figure 5-4.

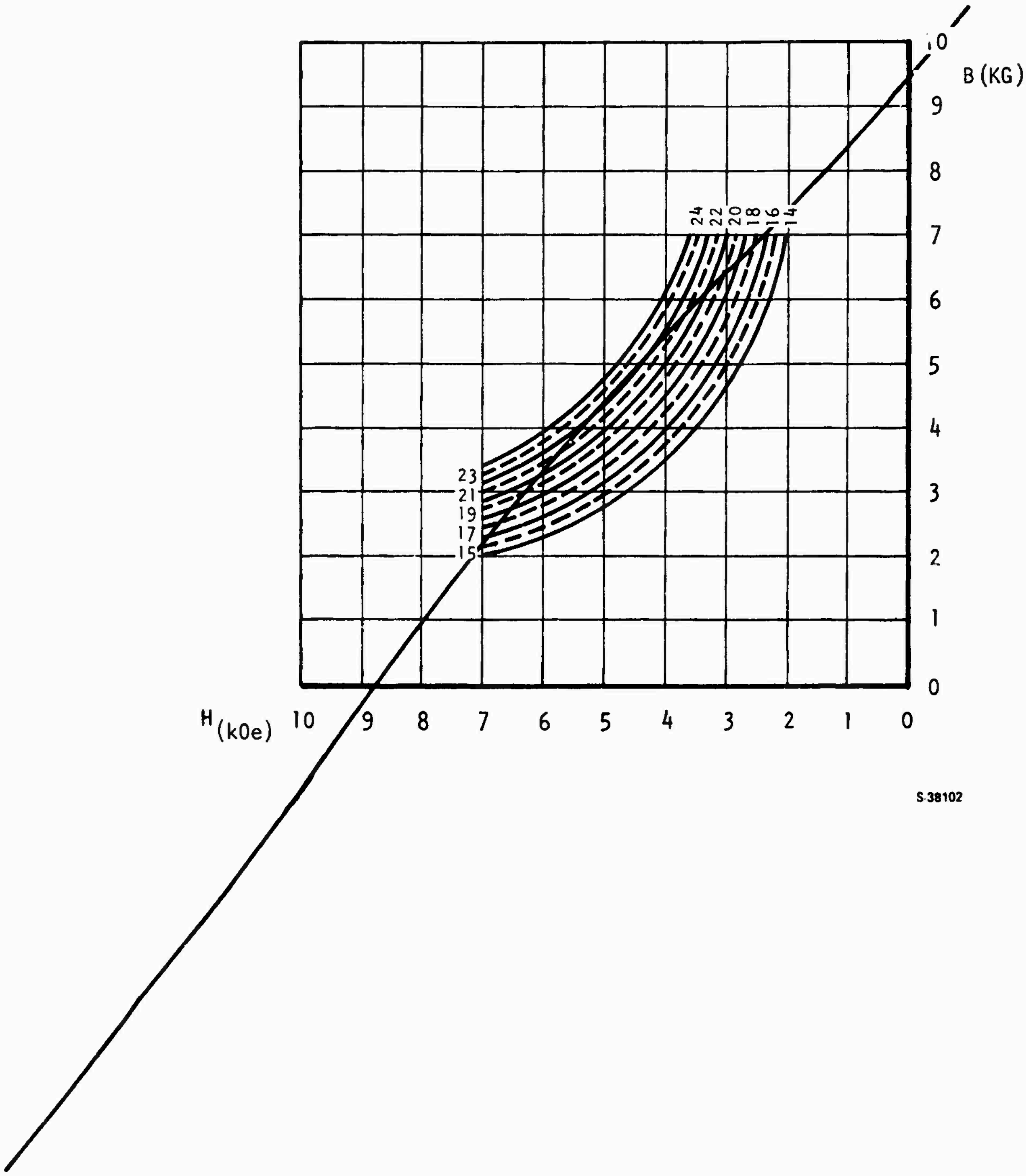
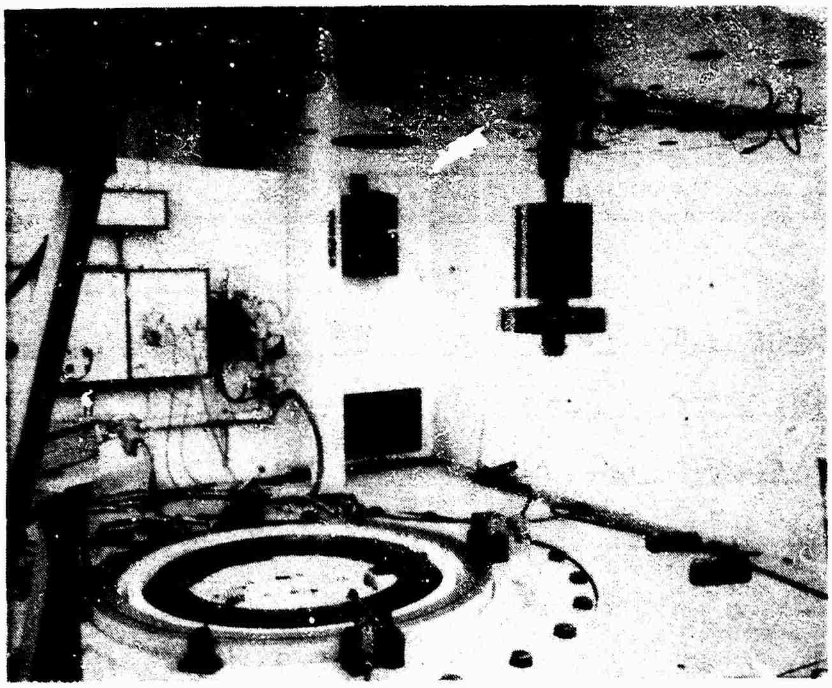
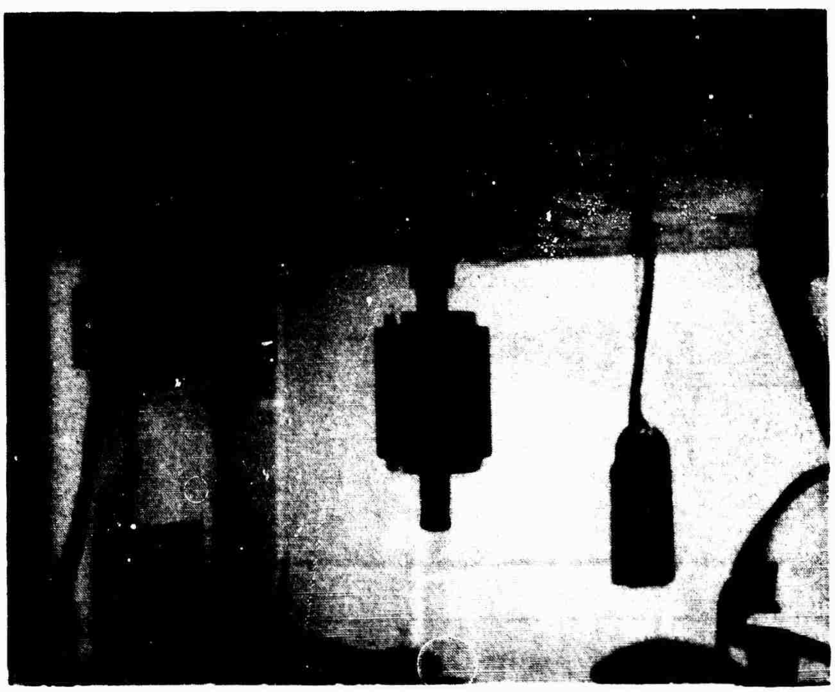


Figure 5-1. Typical Magnet Curve



F-30065

Figure 5-2. HIP-Bonded Rotor in Spin Pit Test Setup (No Magnets, Stabilizing Flywheel)



F-30066

Figure 5-3. HIP-Bonded Rotor-Magnet Assembly in Spin Pit Test Setup

GARRETT

AIRESEARCH MANUFACTURING COMPANY OF CALIFORNIA

LABORATORY TEST LOG

ARTICLE ON TEST P.M.G ROTOR S/N DATE 1-27-78

E.W.O/CHGE. NO. 3400-250443-02-0500 SUPP. I.D.

P/N TECHNICIAN JIM YOKOTAKE DATA SHEET LOG SHEET 172

TIME

ACCELERATE ROTOR TO 33,800 RPM. HOLD FOR 1 MIN

DECEL. TO ZERO

PIT VACUUM 60 MICRONS

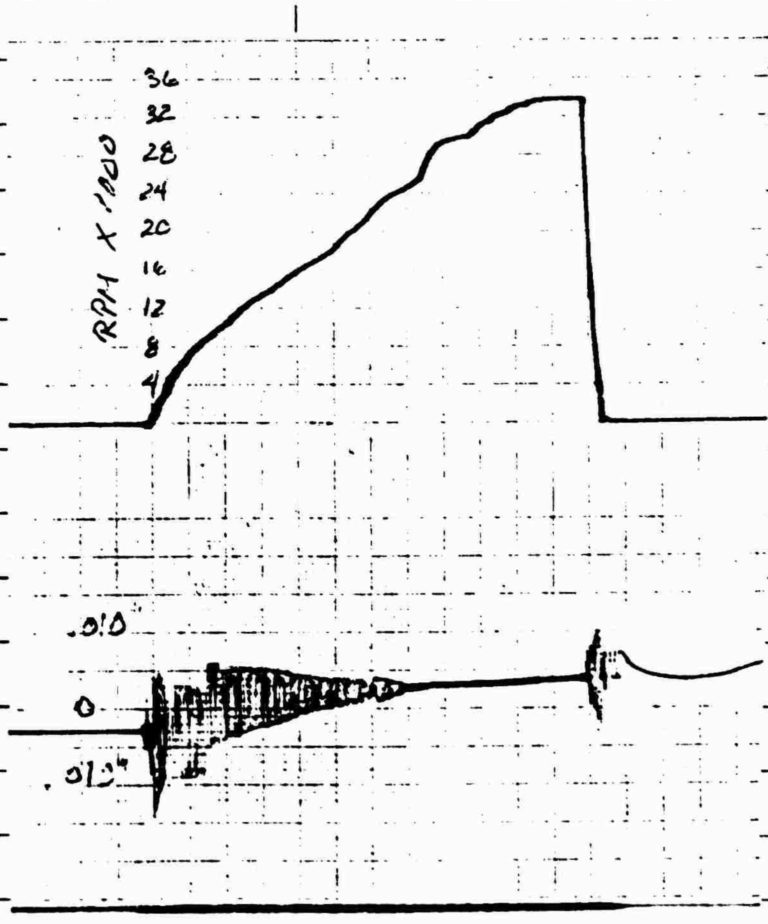


Figure 5-4. Typical Test Data Sheet

Bore Seal

The mechanical integrity of the bore seal is very important from the overall cooling system performance standpoint. The graphite filament-wound tube has to withstand approximately 20 psi inward Coolanol pressure without buckling and leaking. Each part was successfully tested to 25 psig as required by drawing 2046690 (Figure 5-5).

Main Stator Housing

Drawing 2046627 (Figure 5-6) shows the intricate design details. All Coolanol loop passages were leak tested at 150 psig to assure no fluid loss in operation.

Stator Assembly Pressure Drop Tests

Completely varnished and unvarnished specimens were tested to confirm pressure drop calculations. Based on the testing, the final configuration of the stator was established with painted-on HML varnish on the end turns only and no varnish in the slots. Test data is shown in Figure 5-7, which closely agrees with the calculated values shown in the thermal analysis section.

SCR Loop Assembly Pressure Drop Tests

Coolanol 25 flow vs pressure drop tests were conducted for the 12 SCR-heatsink assemblies installed in the main housing. Test data closely followed the predicted performance, as shown in Figure 5-8.

Thyristor Device Screening Tests

Tests were performed as shown in Table 5-1 and described under "Performance Verification of Power Electronics."

GENERATOR CONTROL UNIT TESTS

Lab Tests of GCU Components

The initial design was first checked at the PC board level by means of a PC board test box fabricated in house. This test box consisted of the mating connector wired to break-out points so that the PC board could be stimulated by external lab equipment and outputs could also be measured by lab equipment.

During this open-loop testing it was found that the sync integrator amplifier, Model LM149, was causing too much offset, which in turn caused distortion of the integrated output. This amplifier was replaced with Model LM148, which corrected the problem.

Other functions which were checked open loop were:

- Comparators
- α command
- Logic
- SCR drive - resistive load and with return transformers
- Microprocessor
- I/O conditioning board

Before assembly of the GCU, the individual PC boards and the power supply were checked for correct operation.

The chassis wiring was checked for continuity and comformance to the interconnect diagram.

In order to test the PC boards it was necessary to fabricate a PC board test box. This test box consisted of the mating connector wired to break-out points so that the PC board could be stimulated from external signal sources and circuit responses measured by lab test equipment.

Major areas of additional circuit development required at the PC board test level were as follows:

- Sync integrator amplifier, offset too high; changed from LM149 to LM148
- Sync of logic waveforms required adjustment of sync integrator offset and amplitude; added pot to adjust offset
- Comparator storage time causing delays in logic switch times remedied by changing to higher speed comparator, LM119
- Changes to α command error amplifier gains and dynamic terms to optimize closed-loop frequency response

Test of Completed GCU

The completed unit was tested open loop by means of a system test console, which provided simulated loads for the SCR gate drive circuitry and also had provisions to simulate all the fault conditions. A three-phase variable frequency power supply was used to power the unit for these tests. Most of the testing involved the microprocessor program debugging and hardware integration with the aid of the Microkit development system.

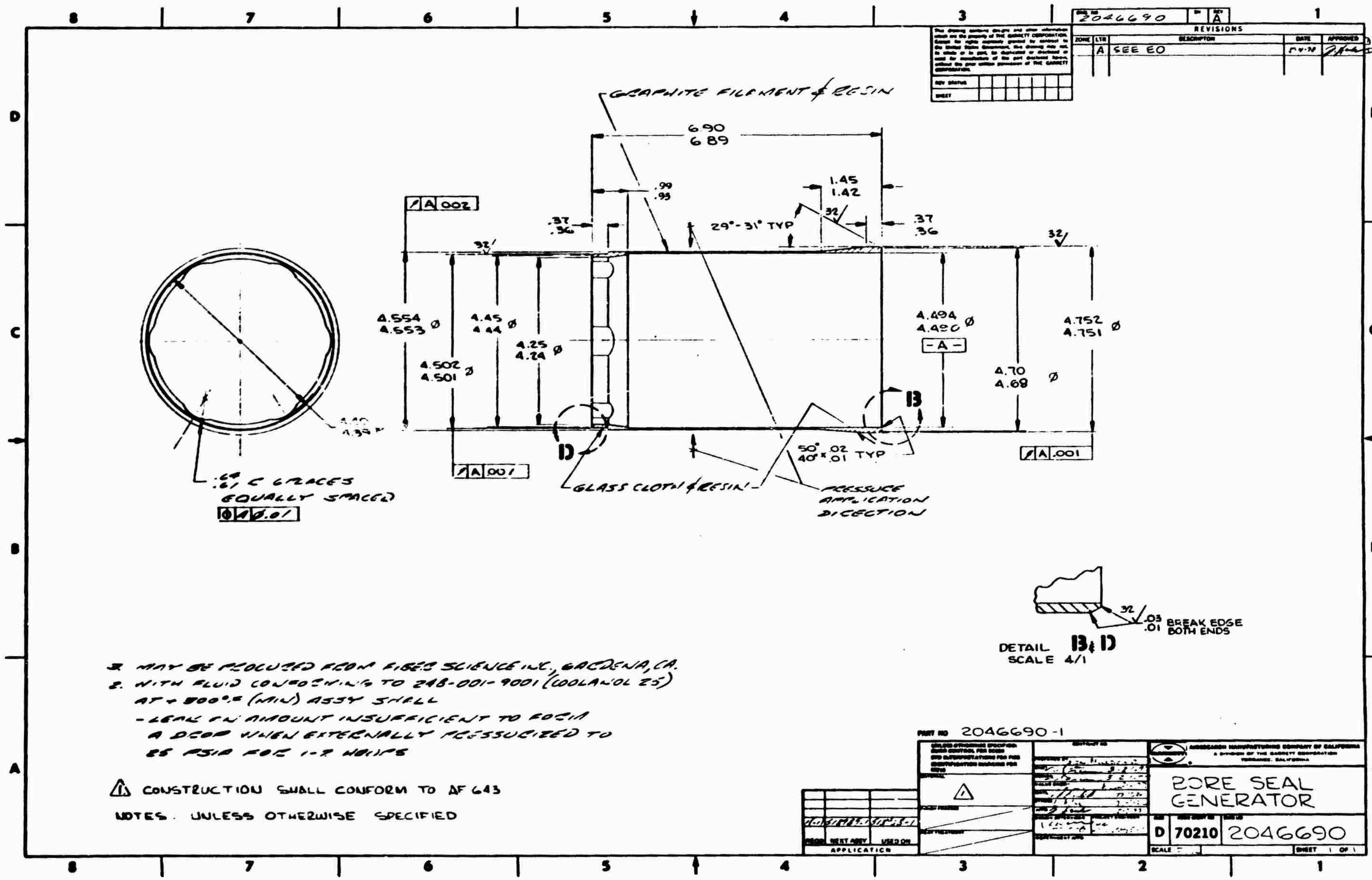


Figure 5-5. Generator Bore Seal, 2046690

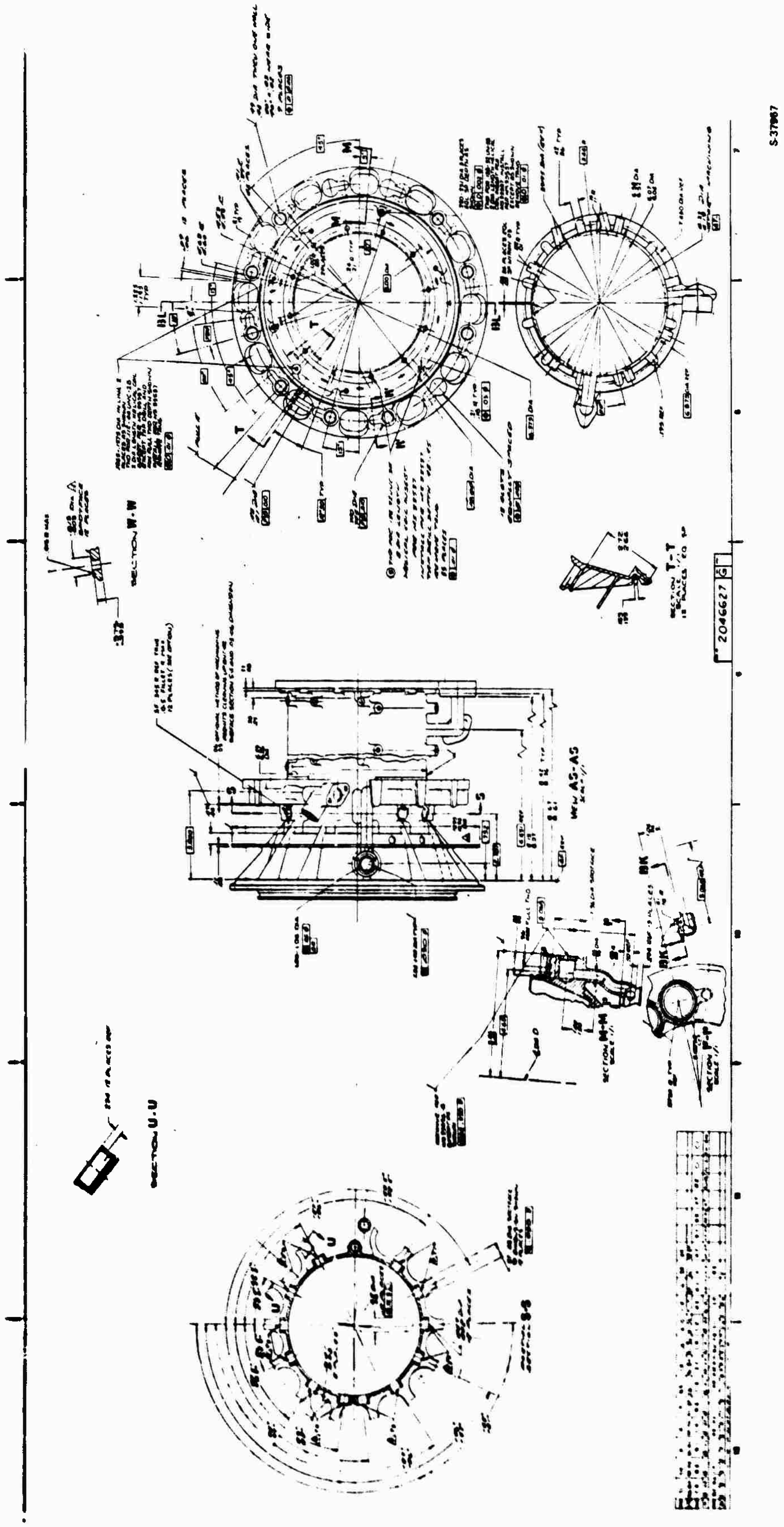


Figure 5-6. Generator Stator Housing Assembly, 2046627 (Sheet 1 of 2)

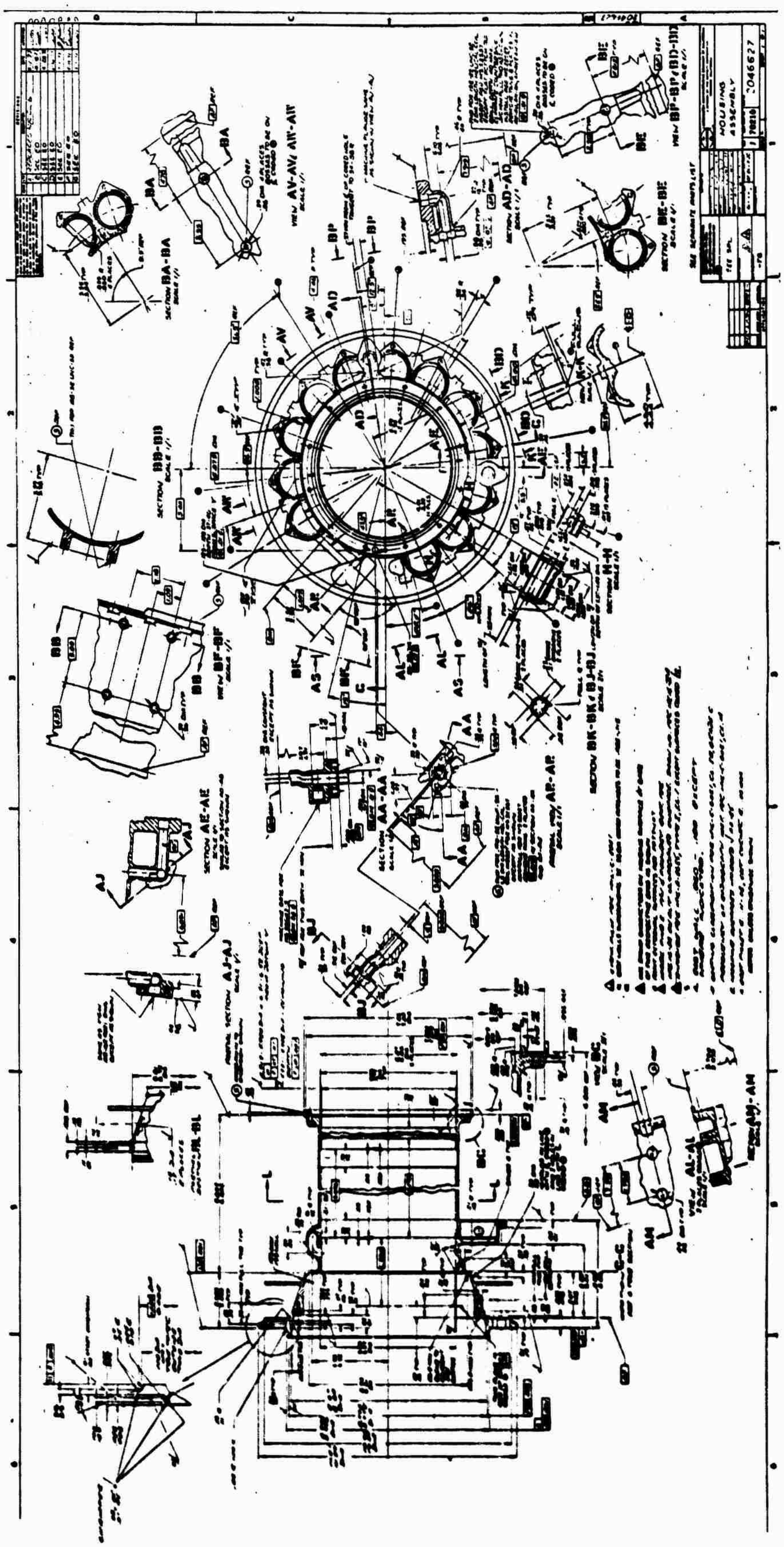


Figure 5-6. Generator Stator Housing Assembly, 2046627 (Sheet 2 of 2)

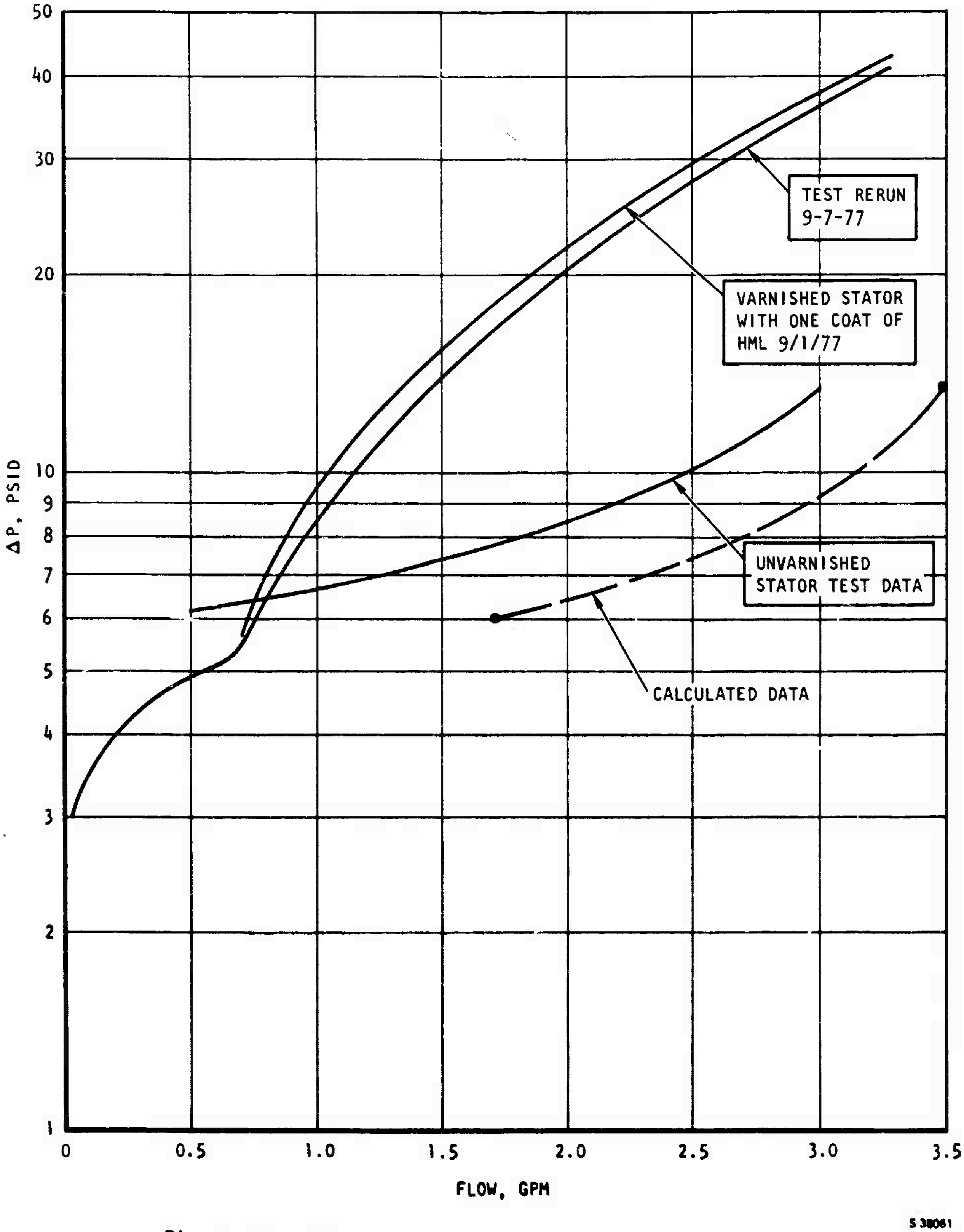


Figure 5-7. Generator Coolanol 25 Flow vs Pressure Drop, Using Stator Mockup Assembly

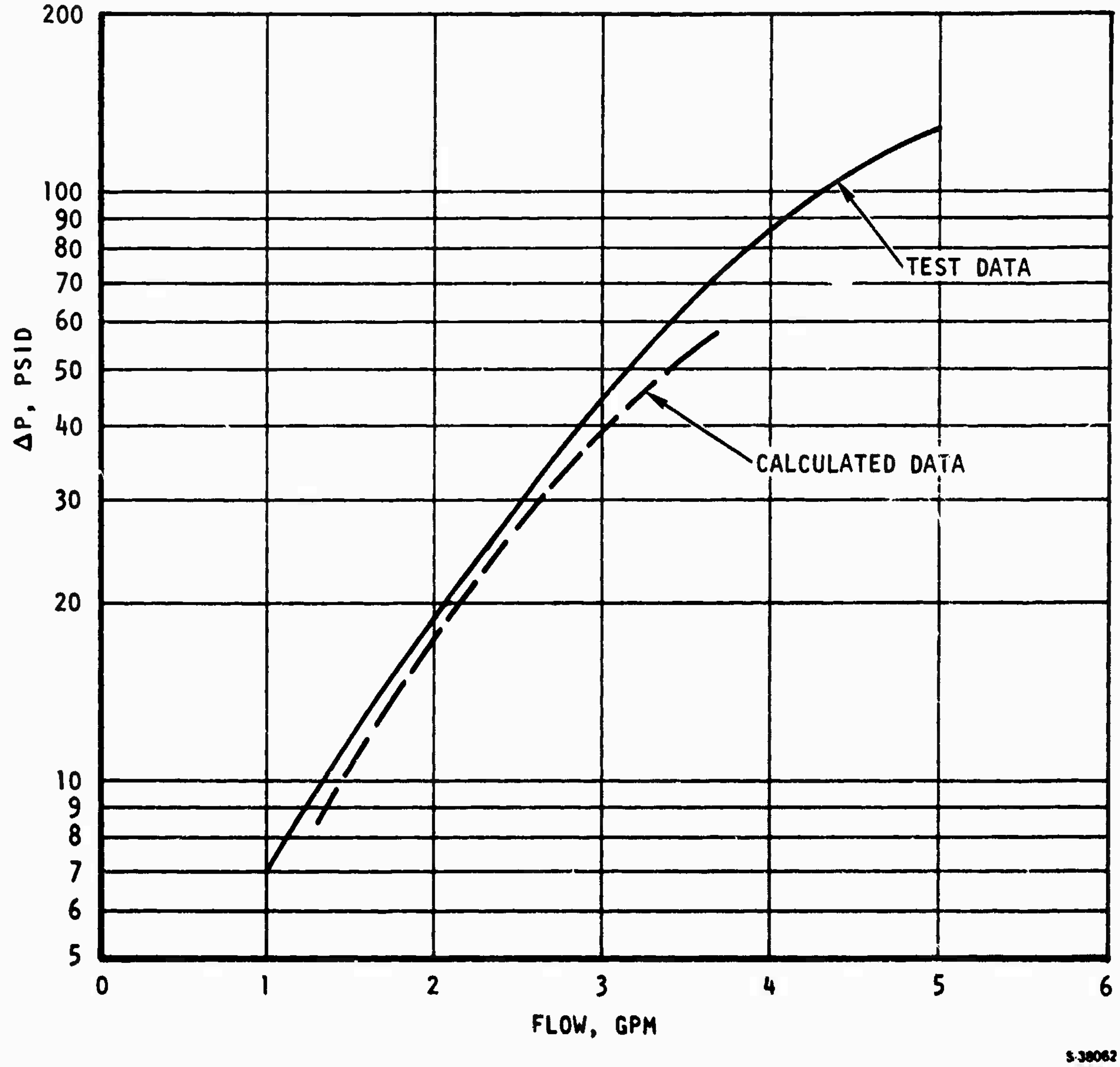


Figure 5-8. Generator Coolanol 25 Flow vs Pressure Drop for 12 SCRs Installed in 2046627-1 Housing

TABLE 5-1

COMPONENT ELECTRICAL TESTS

Component	Insulation Resistance	Dielectric Test	Other Tests
Feed-through capacitor 519668-1	20,000 megohms at 2100 vdc, 25°C	(No test)	Capacitance value Insertion loss Dissipation factor
Ripple capacitor 546309-1	25,000 megohms at 2600 vdc, 25°C	1200 vdc	DC burn-in Thermal shock 600-vac square wave Temperature rise Capacitance value Dissipation factor
Interphase Transformer 2047027-1	2000 megohms at 2500 vdc, 25°C	1500 vac	Winding resistance Proof pressure Leakage check
Ripple inductor 2046650-1	2000 megohms at 2500 vdc, 25°C	1500 vac	Winding resistance Proof pressure Leakage check
Auxiliary stator 2046662	2000 megohms at 2500 vdc	1200 vac	1000-volt surge Winding resistance Field rotation
Main stator 2046627	2000 megohms at 2500 vdc	1500 vac	2000-volt surge Winding resistance Field rotation
Thyristor 546306	See other tests	See other tests	Voltage characteristics Current characteristics Temperature characteristics Gate characteristics Timing characteristics

COMPONENT ELECTRICAL TESTS

Before system interconnection and assembly, all major components in the electrical circuit were subjected to quality assurance testing on the individual basis, as listed in Table 5-1.

Generator-Only Tests

The SCR firing sequence information is derived from the auxiliary winding. In order to properly phase the two stators, the generator was rotated at approximately 1500 rpm by using a hand-held drill motor drive and the main stator No. 1 winding, and the auxiliary stator winding output was aligned by looking at the waveforms on a dual beam oscilloscope. A typical photograph is shown in Figure 5-9, and vector representation of the phase relationships is depicted on the assembly drawing, 518989-1 (Figure 3-2). Alignment of the auxiliary stator involved mechanical rotation on a left-hand fine-thread mount, checking output, and securing in place by using a set-screw after satisfactory alignment had been obtained.

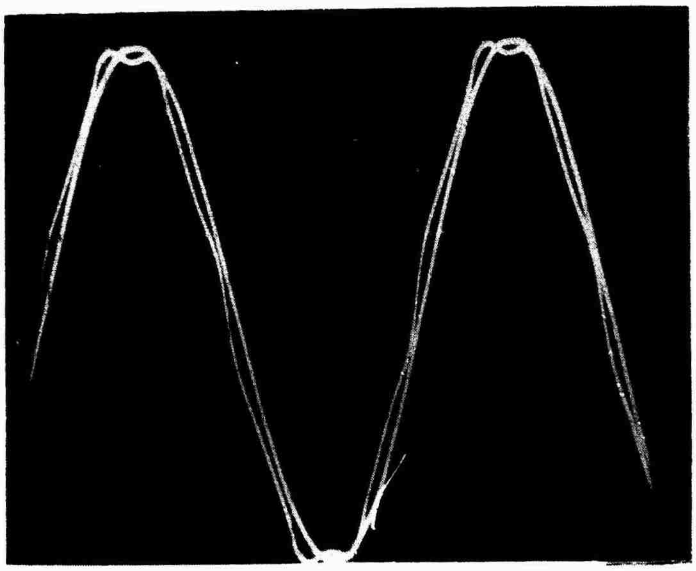
After the generator had been assembled, insulation resistance at 500 vdc and dielectric checks at 1200 vac were performed. Upon successfully passing the static tests, the unit was mounted on the test stand and no-load output voltage checks, mechanical integrity tests to 18,000 rpm, and coolant system capacity development tests were conducted. It was determined that the electromagentic performance and the mechanical integrity of the generator were as predicted. However, the cooling system reservoir had to be enlarged to handle the Coolanol expansion due to heating.

Performance Verification of Power Electronics

Certain tests peculiar to the power electronics were performed to verify component performance. As a result of these tests, the component performance characteristics were verified, with the exception of the Interphase Transformer (IPT), which was determined to be saturating when tested. An IPT with an increased volt-second capability was therefore developed.

The thyristor performance was verified by testing of samples prior to purchasing of devices. Then each of the 36 devices was screened using the same tests, as follows.

Stress screening tests were conducted on each device by raising the junction temperature to the maximum rated temperature, applying rated blocking voltage, and measuring for leakage current stability. For the 270 vdc generator program SCRs were checked for leakage current stability at 175°C with a nominal operating voltage for actual in-service conditions (600 volts).



F-30067

Main Winding: Sinusoidal waveform
Auxiliary Winding: Slightly distorted waveform
Horizontal Calibration: 2 msec/div
Vertical: Set to match amplitude

Figure 5-9. Main and Auxiliary Winding Adjustment Output Waveforms

Thermal stress tests, using SCRs for this requirement from a standard production run, showed the following results:

No. of SCRs	Junction Temp	Blocking Voltage	Hours	Leakage Current
10	150°C	1200 V	450	Stable
10	175°C	1200 V	72	Stable

The above tests were then continued until 1000 total hours of operation at the temperatures indicated were completed. At some higher temperature (above 175°C), the SCRs are subject to random turn-on. When the temperature returns to normal, the SCRs return to normal operation.

The following photographs are examples extracted from test data of the power circuit tests.

Figure 5-10 is a typical thyristor gate drive. The upper trace is an example of gate voltage, while the lower trace is of gate current. Note: the lower trace is inverted.

Figure 5-11 is an example of the dc ripple voltage waveform. No amplitude calibration exists for this measurement. The irregularity of the waveforms tells the story of scattered thyristor firing. After calibration of the firing pulse generator the ripple voltage became more regular. Ultimately, a design modification to the GCU was necessary to correct the deficiency.

Figure 5-12 is the adjusted ripple voltage from one half of the PDR. In this test the circuit was broken at the IPT. Only half of the power converter is operating (note the repetition rate difference between Figures 5-13 and 5-14). Comparison of the two photos indicates trouble in the firing gate circuits and in the IPT.

Figure 5-13 is the ripple current in the inductor of the power converter with the power converter configured with one PDR only. Figures 5-14 and 5-15 are comparison photos. Note the regularity of the unfiltered waveforms.

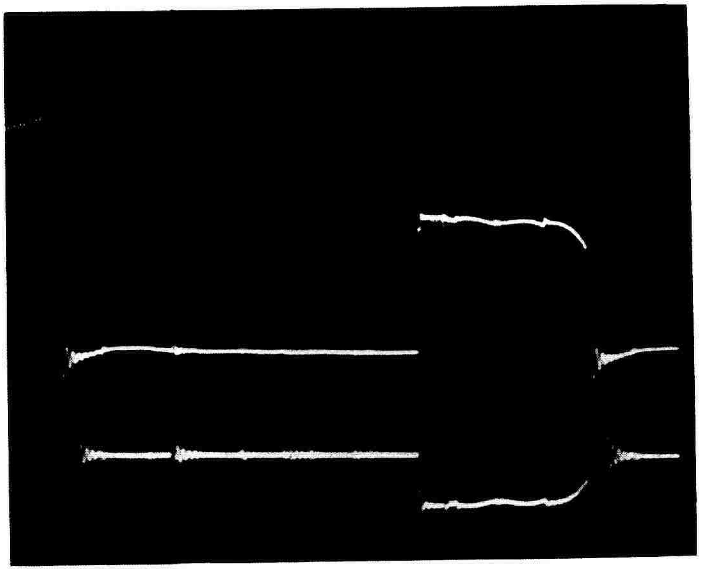
Figure 5-14 is the evidence of IPT saturation which led to IPT redesign. Observe the zero volt steps in the Ø to IPT CT voltage waveform (lower trace).

Figure 5-15 is the phase current waveform to be expected from two phase-shifted PDR's operating in parallel without an IPT.

Figure 5-16 indicates IPT saturation; notice current peaking at discontinued current transitions.

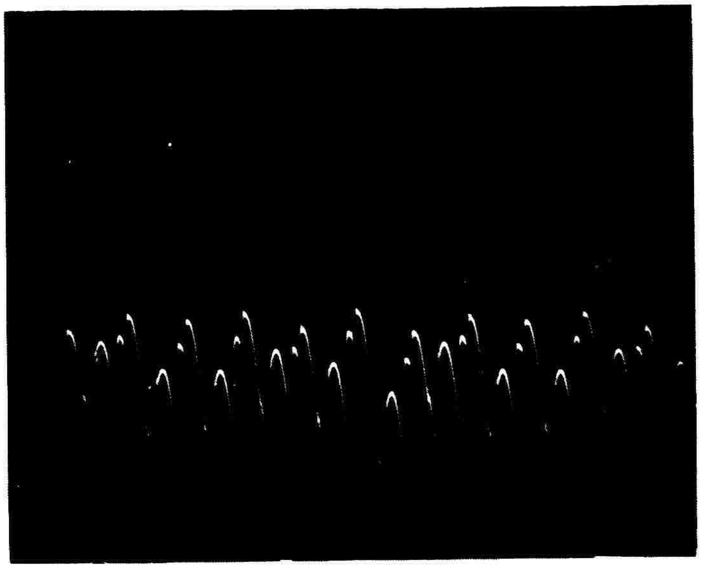
Figure 5-17 is a photograph taken after installation of an IPT of sufficient rating to withstand the volt-second difference of the two power sources.

Figure 5-18 is a photograph of the alternator phase voltage which is typical.



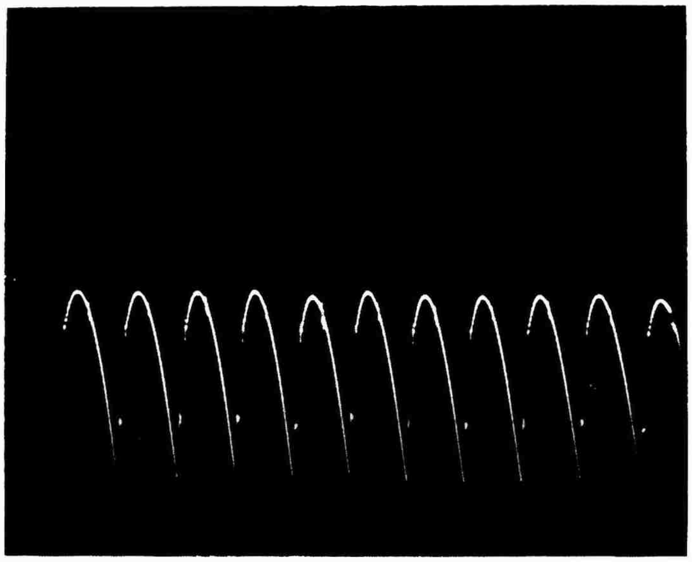
F-30127

Figure 5-10. Gate Voltage and Gate Current Waveforms



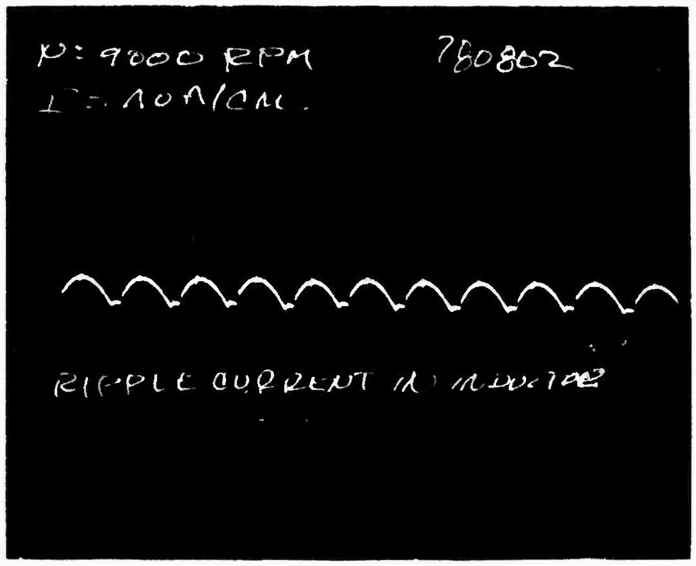
F-30128

Figure 5-11. PDR Output DC Ripple Voltage Waveform Indicating Alpha Scatter



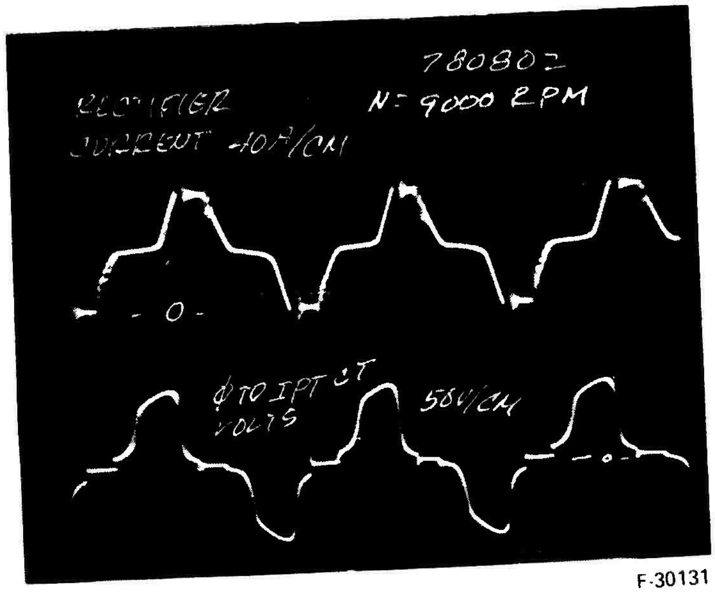
F 30129

Figure 5-12. Ripple Voltage in 1/2 PDR After Adjustment of Thyristor Gate Firing Angles



F 30130

Figure 5-13. Inductor Ripple Current With Balanced Phases



F-30131

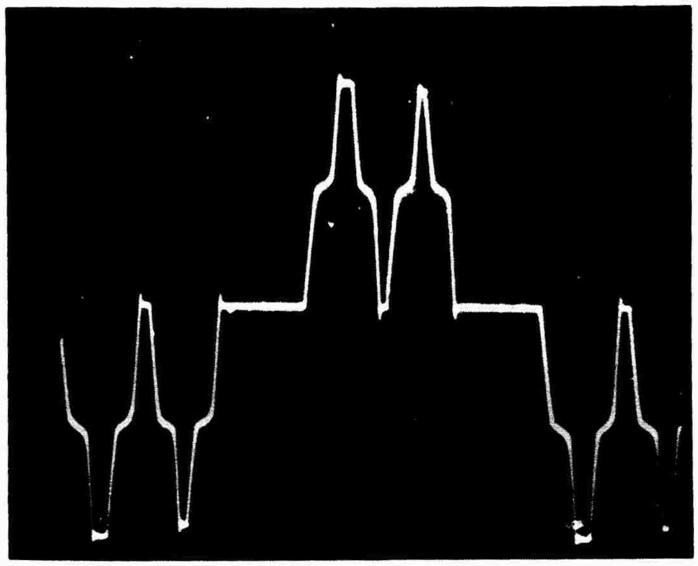
Figure 5-14. IPT Saturation Waveforms

This photograph shows saturation of the IPT about 1/2 way through the cycle. The upper trace is the rectifier current from 1/2 of the PDR. The lower trace is of the IPT voltage center tap to one end. The current waveform (upper trace) is coincidental to the voltage zero of the lower trace and occurs because the IPT saturates, permitting shoot-through. Discontinuous phase currents will result.

F-30132

Figure 5-15. Two Phase-Shifted PDRs in Parallel Without an IPT

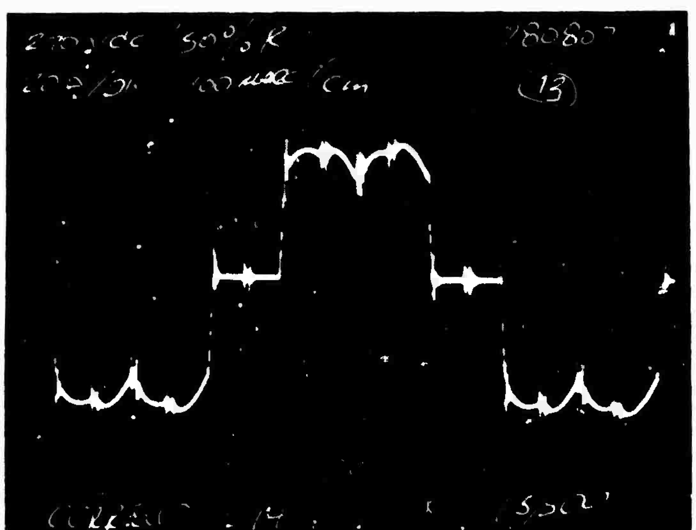
The above photo shows the phase current in one phase of two phase-shifted PDRs which are connected together without benefit of an IPT. Note that current flow is discontinuous.



F-30133

Figure 5-16. IPT Saturation and Current Peaking

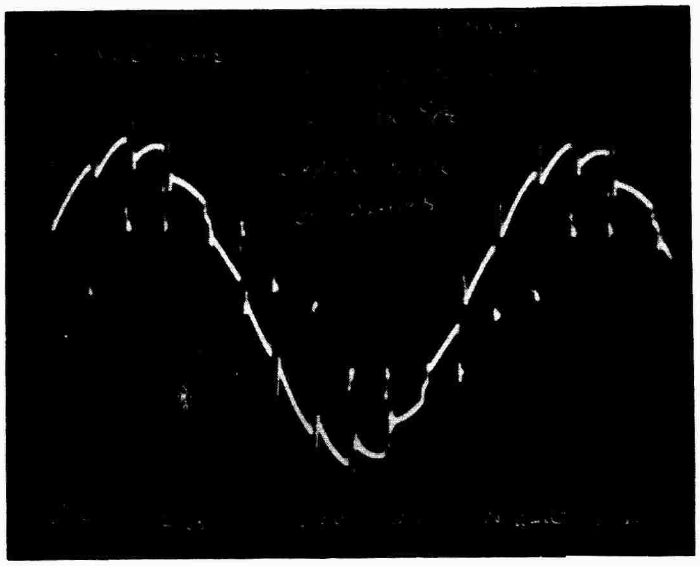
The photo above is typical of phase current in a converter using two phase-shifted PDRs which are connected together with an IPT having insufficient volt-second capability. Current flow is discontinuous.



F-30134

Figure 5-17. Normally Functioning PDR with Properly Designed IPT

This photograph represents the phase current and is typical of each of the six alternator phase currents with a normally functioning PDR operating at one-half load, connected together with a properly designed IPT.



F-30135

Figure 5-18. Typical Alternator Phase Voltage

This photograph is representative of phase voltage, line-to-line, at the alternator terminals. The spikes on the waveform are the result of commutation overlap, a phenomenon that occurs as a result of alternator sub transient reactance which causes overlap of the turn-on and turn-off of the PDR thyristors. The result is finite duration phase-to-phase short circuits.

SUBYSTEM DEVELOPMENT AND TESTING

Pitot Pump

The separate pitot pump test rig shown on drawing SK72479 (Figure 5-19) was built to finalize the pitot pump component configuration and internal plumbing connections. The development pump assembly was tested several times with minor internal modifications involving fluid passage hole enlargement, drag cup vane alignment, closer vane clearances, and sump-to-reservoir connection variations. The final design performance curves are shown in Figure 5-20.

Quick-Disconnect

To comply with the specification requirements, a high-speed decoupler was designed as shown in Figure 5-21. Referring to the diagram, operation of the mechanism is as follows:

Energizing the solenoid disables the latch, permitting the actuator to rotate. Under the influence of the brake springs and inclined planes, the actuator rotates and the brake plates translate, engaging similar brake surfaces which are integral with the Acme nut.

The resultant retarding torque tends to slow or stop the Acme nut rotation; however, the drive shaft/screw continues to rotate at engine speed. The consequent differential motion is sensed by the screw-nut combination, thus producing axial motion of the drive shaft and eventual disengagement.

The hardware was assembled into the generator and all adjustments were made to design clearances and travels. The generator was driven by a hand-held drill motor at approximately 1500 rpm and the solenoid was momentarily energized. The decoupler operated satisfactorily several times. Decision was made to leave the mechanism in the generator for the electrical tests, but no high-speed quick-disconnect operational tests were planned until electrical system development was completed.

During 18,000 rpm testing, brake plate mounting flanges fatigued and caused unsymmetrical loading on the actuator, resulting in decoupler false trip and malfunction. Photographs of the failed parts are shown in Figures 5-22 through 5-25. Due to program funding limitations, decision was made to remove the quick-disconnect feature from the first unit.

Major refurbishment of the unit consisted of the following:

- Rewind stator assembly on same stack
- Replace all bearings
- Install new bore seal
- Install new gate drive assembly circuit board
- Rework rotor assembly

- Clean up main housing, install new feed-through terminals
- Recheck and remachine end bells
- Check out all thyristors
- Reassemble unit without brake plates, actuator, balls, brake springs, solenoid and latch.

SYSTEM TESTING

After successful completion of component and subsystem development, the 270 vdc system was set up and interconnected as shown in Figures 5-26, 5-27, and 5-28. System integration tests were conducted to achieve the following major program objectives:

(a) Meet ripple voltage requirements

(b) Meet transient response requirements

(c) Meet steady-state voltage regulation requirements

(d) Provide automatic start-up/shut-down and protection

The objectives were accomplished by open-loop and closed-loop system operation, resolving the following development problem areas:

(a) Thyristor firing timing (alpha scatter)

(b) Power supply filtering effects

(c) Loop stability

(d) Interphase transformer saturation

(e) Microprocessor software and hardware integration.

The testing and the final results are discussed in detail in the following paragraphs.

THYRISTOR FIRING TIMING

Tests on the machine showed that there was a high ripple content on the 270V output, especially at low loads. Examination of the output ripple waveform showed that the individual SCRs were not firing at even intervals as shown in the trace (Figure 5-11). Examination of the logic waveforms confirmed the suspicion that there was in fact asymmetry in the basic firing pulses. This asymmetry was traced to the comparator output were the comparision of alpha (α) command and the synchronizing waveform is made. It was found that the asymmetry was due to two factors: (a) distortion of the synchronzing waveform and (b) variation in storage time of the comparators.

The distortion of the sync waveform was caused by loading effects on the integrator output and also the alpha limit differentiator sum point.

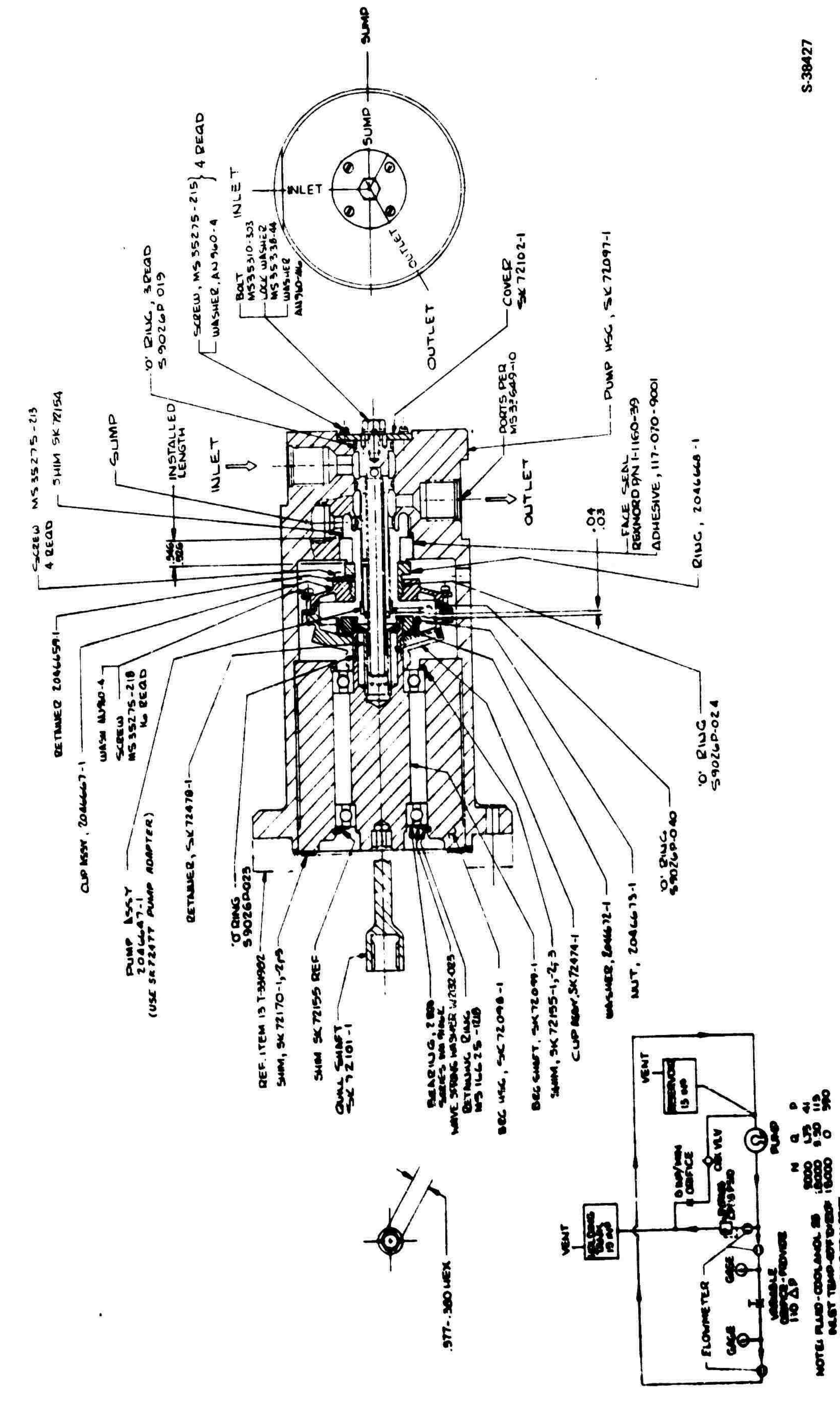
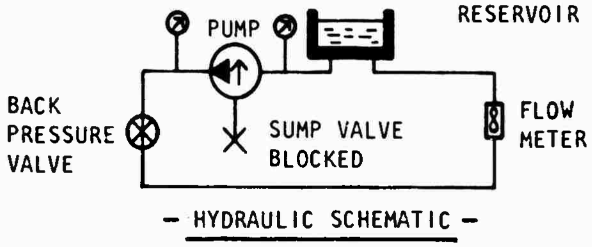


Figure 5-19. Pitot Pump Test Fixture, SK72479



NOTES

1. DATA TAKEN WITH SUMP PORT BLOCKED AND PITOT PUMP PICKUP TUBE VERTICAL UP
2. VANE TO PICKUP TUBE CLEARANCE APPROX 0.030

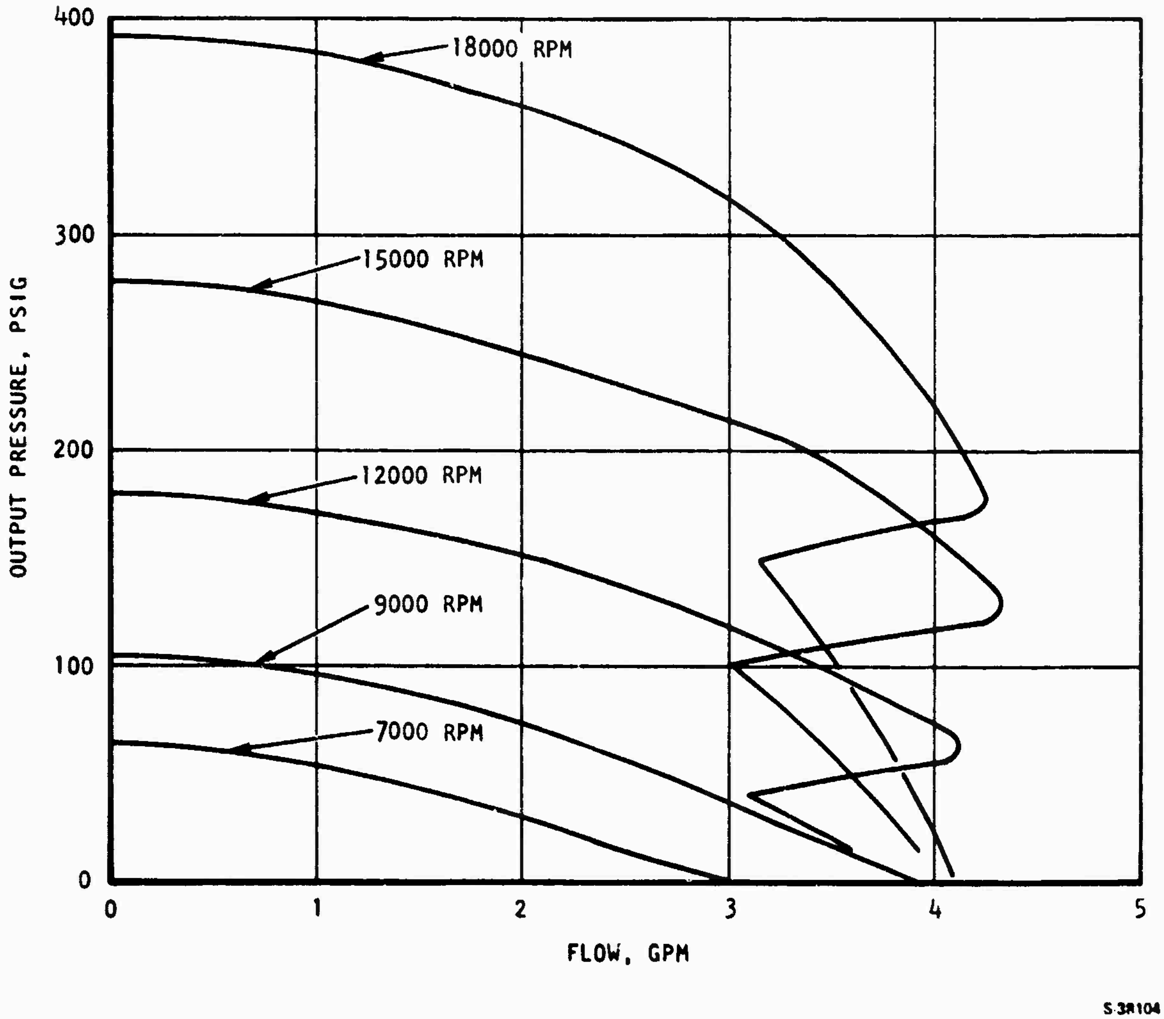


Figure 5-20. 270 VDC Generator Pitot Pump Performance Curves at S/L, R/T Ambient, Using Test Rig SK72479

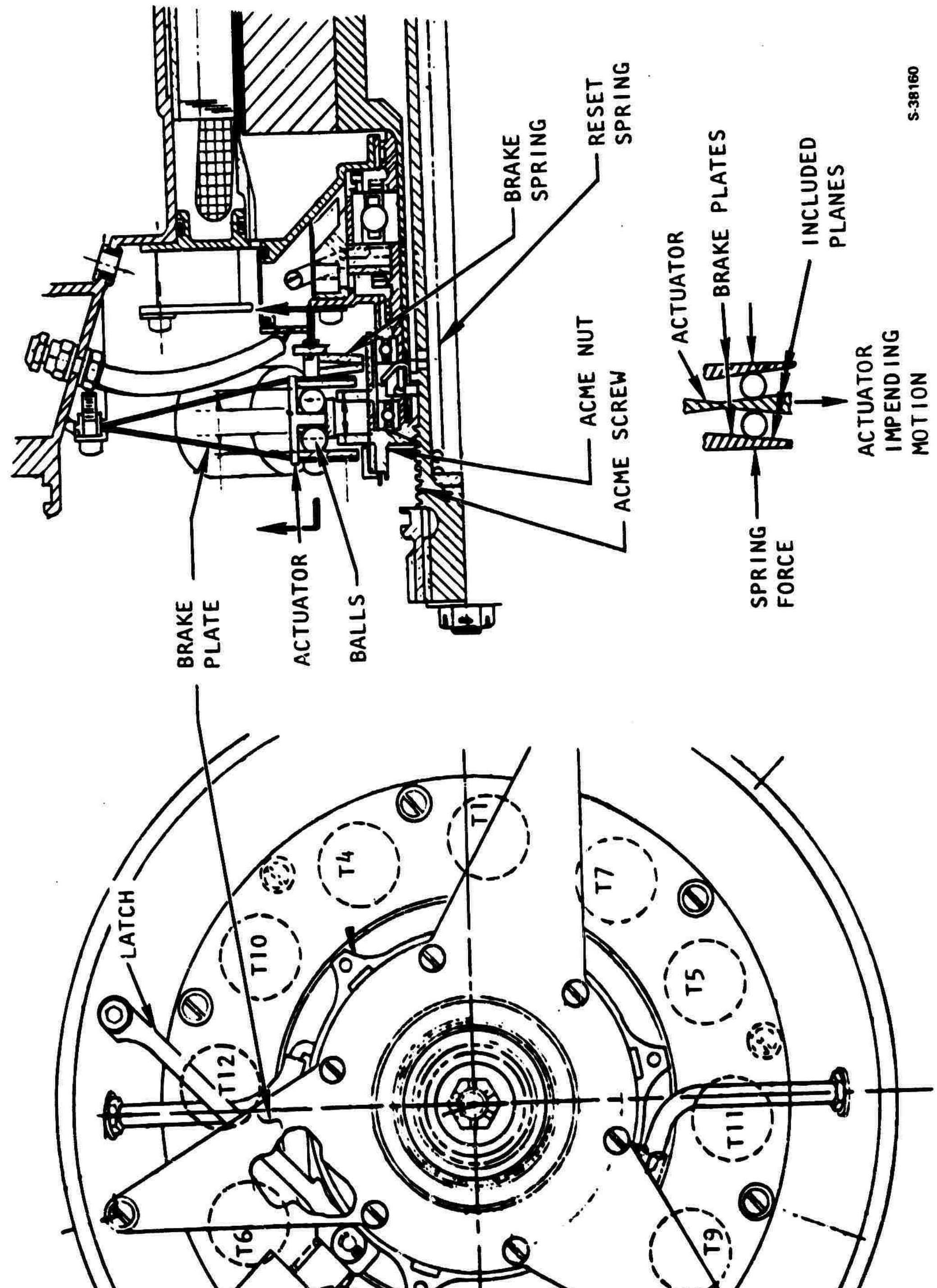
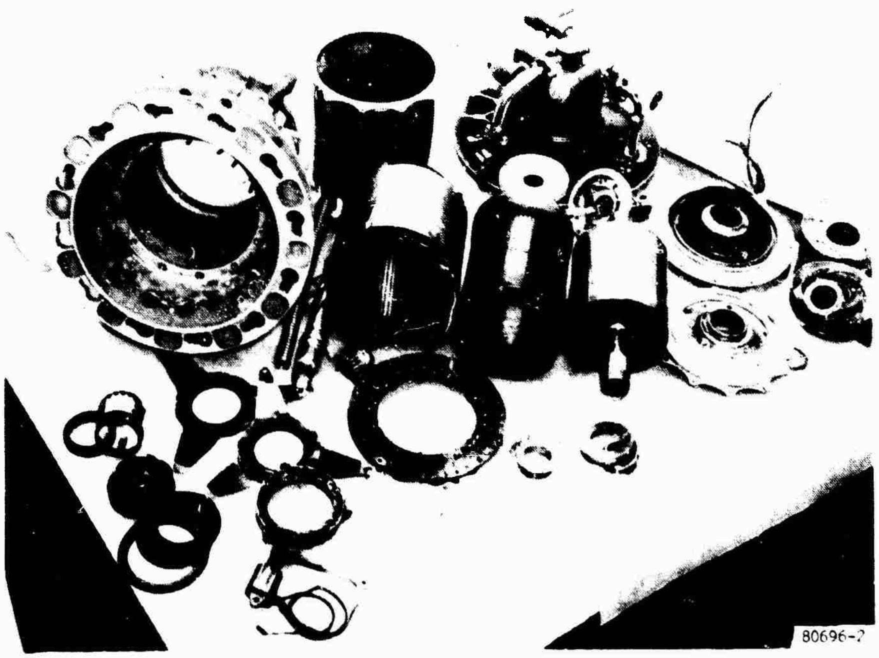


Figure 5-21. Disconnect Arrangement

Figure 5-22. Generator Detail Parts After Quick-Disconnect Failure (View A)



F-30070

Figure 5-23. Generator Detail Parts After Quick-Disconnect Failure (View B)

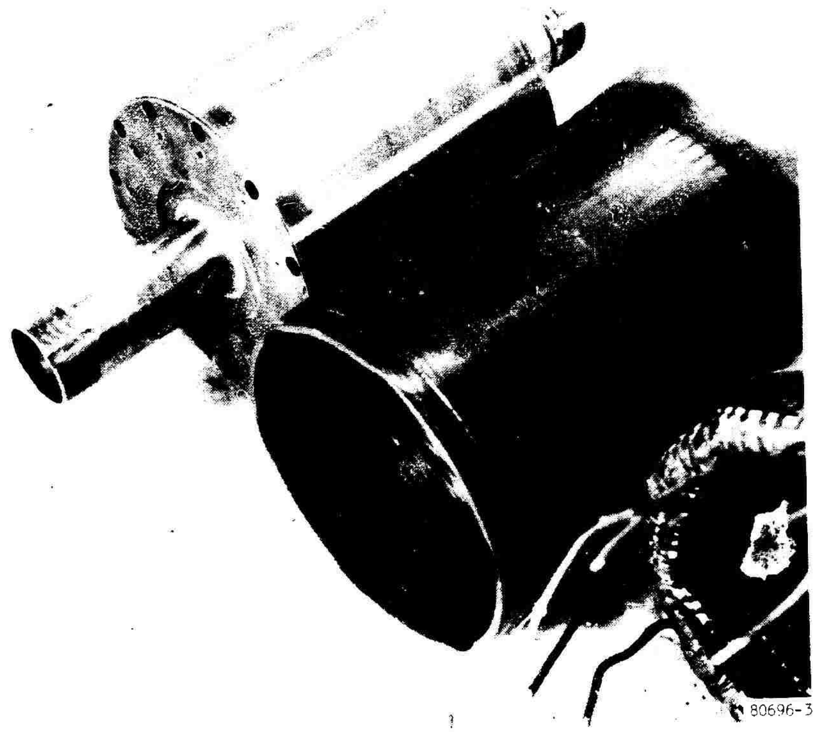


Figure 5-24. Rotor Assembly, Bore Seal, and Main Stator After Quick-Disconnect Failure

80696-4 **F-30071**

Figure 5-25. Quick-Disconnect Detail Parts After Failure

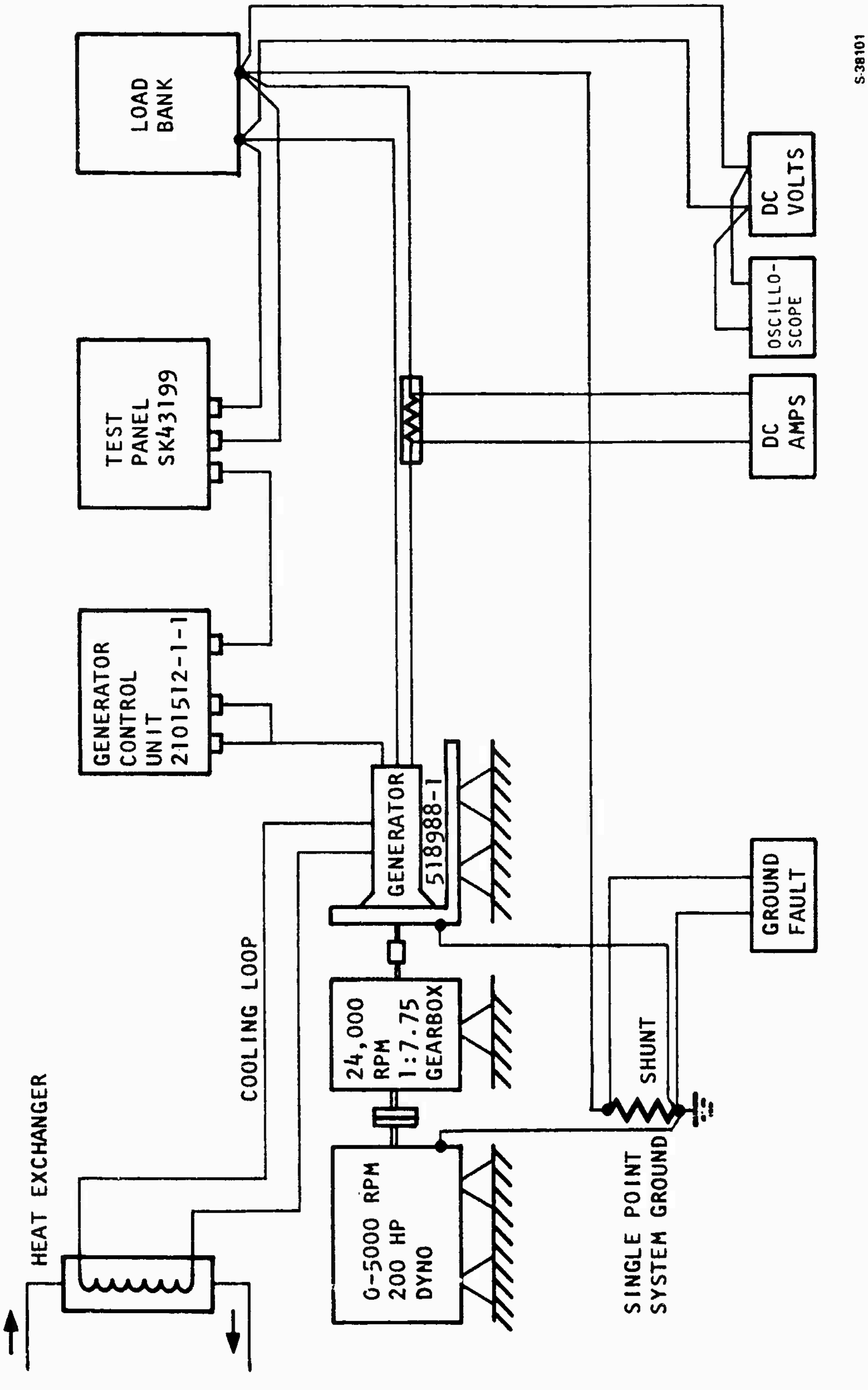


Figure 5-26. Schematic of 270 VDC System Interconnection and Instrumentation

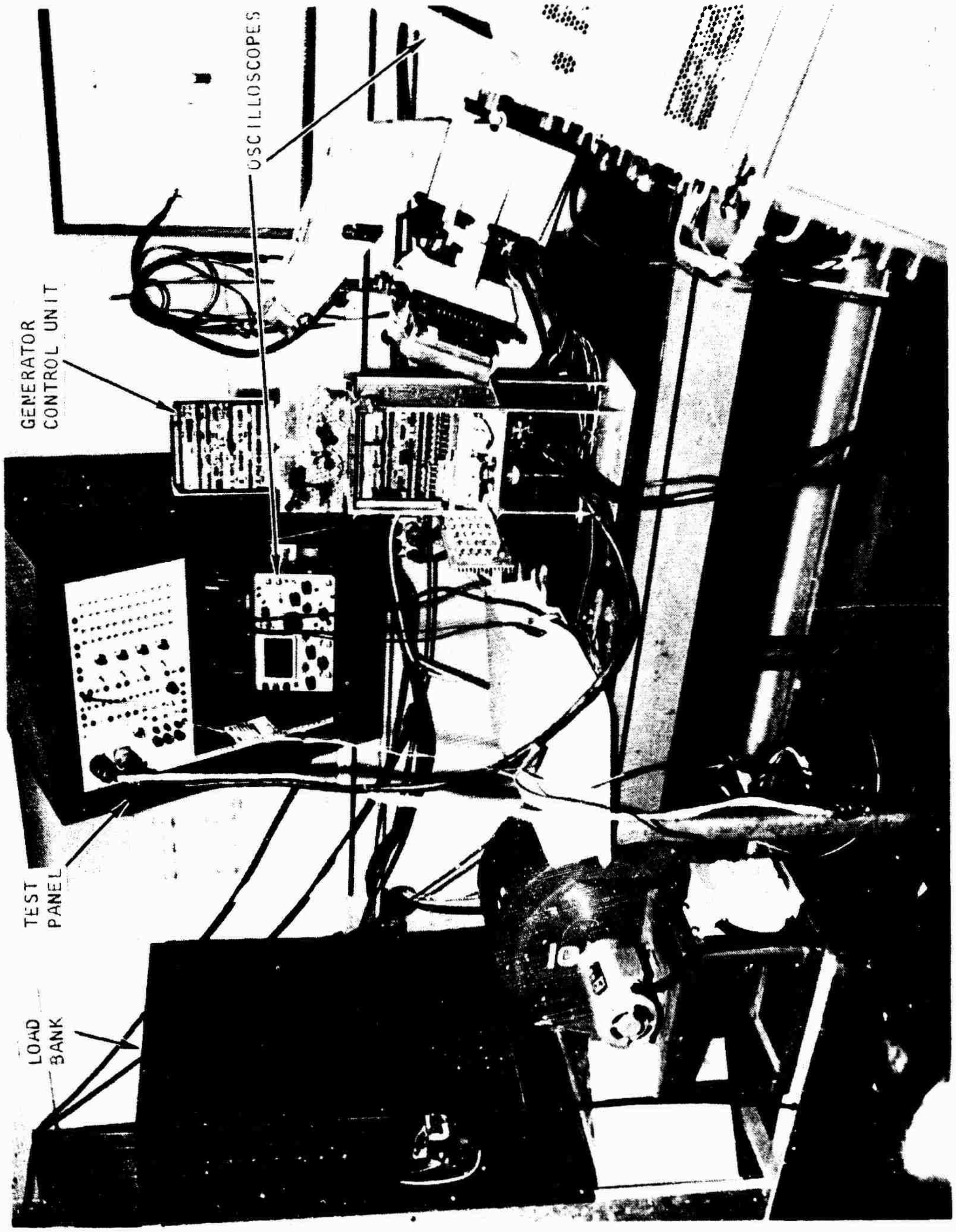
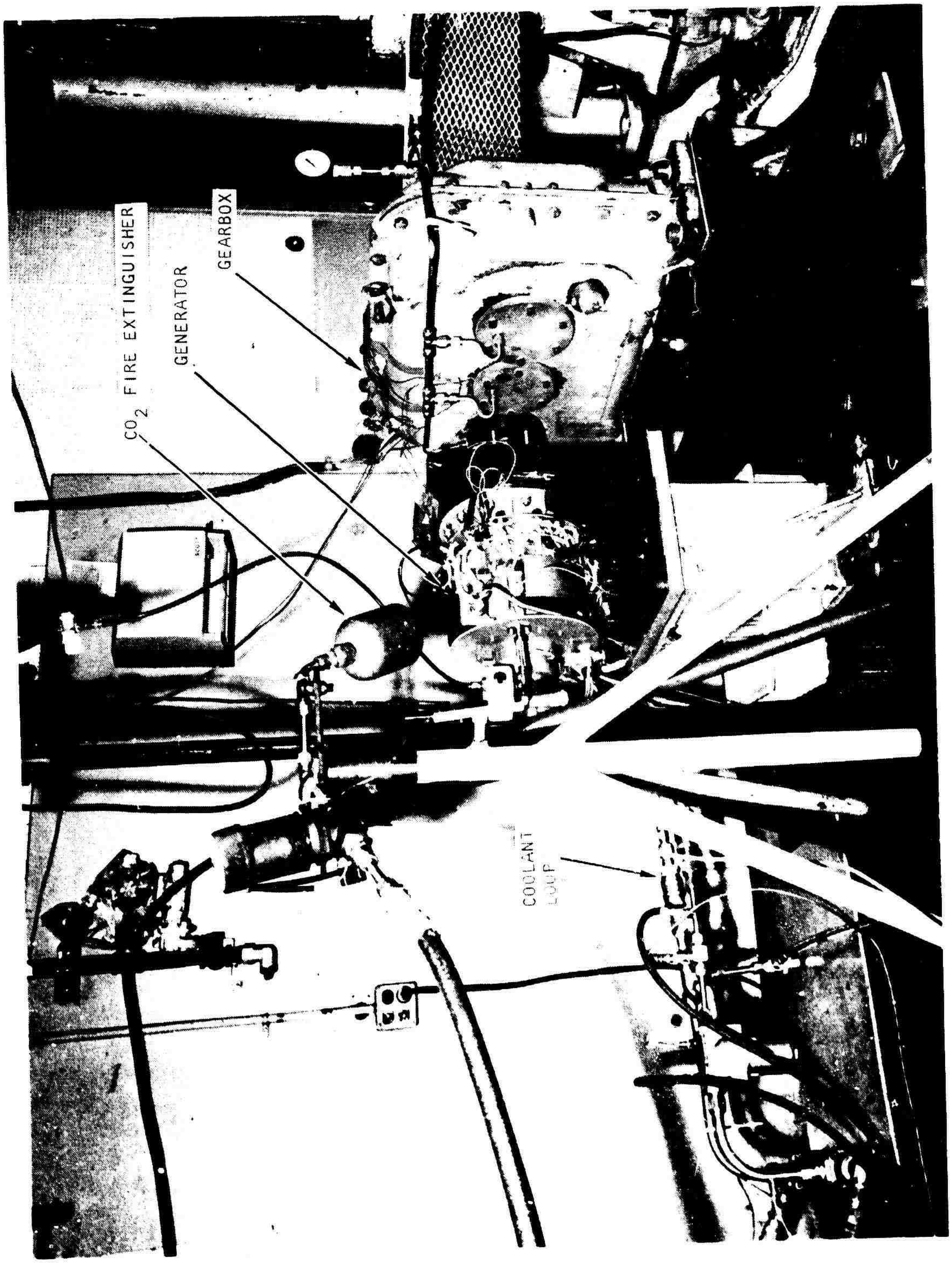


Figure 5-27. Generator Control Unit and Instrumentation Setup



F-30072

Figure 5-28. Generator Test Setup

This area was redesigned using a higher speed comparator (LM119) and limiting the swing of the comparator output voltages. Figure 5-29 shows the comparator outputs before the redesign.

POWER SUPPLY FILTERING EFFECTS

The GCU is powered by an auxiliary winding from the main generator. This 3-phase input is first filtered by an EMI filter before being rectified and regulated to produce control level voltages of ±12V, ±5V and 270V instrumentation power. During initial testing with the machine the EMI filter capacitors overheated due to high-frequency components on the waveform from the machine. An interim design change has been made to replace the EMI filter with discrete capacitors with a higher ripple rating.

+5V POWER SUPPLY FILTER

Initial system testing showed that noise was present on the logic power supply. Further filtering was added on each PC board. Critical items such as the microprocessor chip and PROM were filtered by the addition of high-frequency capacitors at the device power input terminals.

LOOP STABILITY

Preliminary tests of the generator voltage regulator utilized a proportional control system. This control produced an unacceptable voltage drop. The control mechanization was changed to a proportional plus integral control and developed at the highest gain point of the machine, which was maximum speed low load.

The voltage overshoot on load removal was found to be out of specification. This overshoot was due to the stored energy in the filter inductor and could not be controlled by the regulator loop. A clipper circuit was designed and developed to clip the transient overshoot to 350 vdc. This circuit was incorporated into the test box.

MICROPROCESSOR (SOFTWARE AND HARDWARE INTEGRATION)

The MICROKIT 8116 development system was used as a tool in developing software and hardware for the GCU. The system comes with a text editor, an assembler and a monitor. The text editor was used to create and modify source files, and the assembler was used to produce a listing and an object code.

In the initial development stages, there was no GCU hardware hooked up to the MICROKIT system. The GCU software was exercised with the help of the monitor and many bugs were thus eliminated from the software. Later the GCU hardware was hooked up to the MICROKIT with an emulator plug which plugged into the 8080 microprocessor socket on the microprocessor board of the GCU. The GCU software was then exercised with the GCU hardware environment.

The emulator provided the capability of disabling or enabling selective parts of the GCU hardware, thus making possible step-by-step checking of the hardware. Some additional software bugs were found and eliminated at this stage. With the hardware and software fully debugged, the program was transferred into an EPROM. The emulator was then disconnected and the 8080 CPU was plugged into its socket.

F 30374

Figure 5-39. Comparator O[illegible]

FINAL GENERATOR ACCEPTANCE TESTING

Final performance verification tests were conducted on the completed 270 vdc system in the presence of Mr. Joseph Segrest of NADC before shipment. Lab data sheets, Figures 5-30 and 5-31, summarize the actual data taken. Calculated heat loss and efficiency values are also shown. Due to funding limitations, all testing was conducted at room temperature, sea level ambient for both the generator and the control unit.

Due to problems with the telemetry type in-line torque sensor, efficiency values were approximated by using coolant heat loss data, and cross-checked by using dynamometer input power and gearbox efficiency. The small discrepancies shown are due to the fact that no allowance was made for surface heat loss and thermal capacity, and no accurate gearbox calibration data is available.

Typical heat loss and efficiency calculations are shown for test point No. 26 at 17,600 rpm, full load. Properties of Coolanol 25 are obtained from Figure 4-4.

$$\text{Heat loss, Btu/min} = (\text{gpm})(\ \text{T°F})(C_p)(\ )$$

$$\text{watts} = \frac{(\text{Btu/min})\ (60)}{(3.413)}$$

$$\text{At point 26, Btu/min} = (4.6)(19)(0.496)(7.24)$$

$$= 313.9 \text{ Btu/min heat rejection}$$

$$\text{watts} = \frac{(313.9)\ (60)}{(3.413)}$$

$$= 5{,}518 \text{ watts loss}$$

$$\text{General output} = (270)(153) = 41{,}310 \text{ watts}$$

$$\text{Total Input} = 41{,}310 + 5{,}518 = 46{,}828 \text{ watts}$$

$$\text{Efficiency} = \frac{41{,}310}{46{,}828} = 88.2\%$$

Dynamometer input to gearbox : 69.17 hp

Assumed gearbox efficiency : 91%

Gearbox power input to generator : 62.95 hp or 46,960 watts

$$\text{Efficiency} = \frac{41{,}310}{46{,}960} = 88\%$$

The two efficiency values are in close agreement. The final ripple voltage and transient response performance is shown on oscilloscope photographs (Figures 5-32 through 5-34), and graphs (Figures 5-35 and 5-36).

FORM #1330A
AIRESEARCH MFG.

LAB DATA SHEET

Page 1 of 2

EWO 3400-250443-01-0500 DATE 3-28-79 TEST PURPOSE 270 VDC GENERATOR PERFORMANCE

P/N 518988-1-1 BAROM LAB AT SEA LEVEL, ROOM TEMP AMBIENT

S/N R-1 TEMP LAB TEST PERS. S LEE, J DENK, R WATER, B. PASKO, AK, S. BOSAZ
J. SEGREST N.A.D.C. / E.F. ECHOLS

TEST POINT	TIME OF DAY	GENERATOR INPUT SPEED R.P.M.	GENERATOR INPUT TORQUE IN-LB	GENERATOR INPUT HP	GEAR BOX INPUT SPEED RPM	GEAR BOX INPUT LB-FT	GEAR BOX INPUT HP	GENERATOR OUTPUT DC VOLTS	GENERATOR OUTPUT DC AMPS	COOLANT (COOLANOL 25) PRESS. OUT PSI	COOLANT PRESS IN PSI	COOLANT FLOW #/GPM	COOLANT TEMP IN °F	COOLANT TEMP OUT °F	GENERATOR BEARING REAR TEMP °F	GENERATOR BEARING FRONT TEMP °F	CALCULATED GENERATOR η BASED ON HEAT LOSS	CALCULATED GENERATOR HEAT LOSS BTU/MIN	CALCULATED GEAR BOX η %	CALCULATED GEN. η BASED ON GEAR BOX EFF.
NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		REMARKS			
1	1005	9040	383	47.70	1168	51.3	17	270	38	52	47	585/2.5	82	86	105	87	94.6	33.8	91	88.9
2	1011	9040	410	58.81	1166	95.3	31.14	270	76	53	48	592/2.5	89	95	128	95	95.8	50.6		97.1
3	1014	9030	510	73.0	1165	141.2	46.98	270	116	53	48	598/2.6	94	102	134	101	96.2	70.6		98.2
4	1017	9010	594	84.92	1156	190.0	63.73	270	153	55	50	614/2.6	99	108	145	108	96.7	79.7		97.0
5	1025	9010	547	78.2	1161	190.0	67.00	270	153	58	54	625/2.7	116	130	180	130	94.7	130.9		97.0
6	1030	9030	504	72.2	1168	188.5	62.88	270	153	60	55	626/2.7	122	137	202	138	94.3	140.8		96.8
7	1035	9030	509	72.9	1165	189.7	63.12	270	153	59	54	617/2.6	127	144	217	145	93.8	156.0		96.4
8	1040	9050	490	69.9	1168	188.8	62.98	270	153	57	52	616/2.6	129	145	223	147	94.2	145.0		96.6
9	1047	9060	470	*	1168	188.5	63.88	270	153	54	50	608/2.6	130	148	228	149	93.4	165		96.8
10	1053	NOTED FLASH BETWEEN IPT INPUT WIRES & GROUND SHLD OF SCR																		
11		GATE DRIVE CABLE IN CLOSE PROXIMITY / INSTALLED SHRINK SLEEVING																		
12		ON ALL IPT LEADS - IPT O.K. WITH 500 VDC INSUL. RES. ≠ ∞																		
13	1155	18000	270		2319	106	69.93	270	153	140	128	1038/4.4	120	130	200	130				
14	1200	18000	274		2322	105.5	69.96	270	153	137	127	1087/4.5	155	172	270	176	93.4	273.9		87.0
15	1204	DOWN		*																
16																				
17	* NOTE																			
18		TELEMETRY TYPE TORQUE SENSOR DATA IS NOT USABLE DUE TO LARGE																		
19		AMOUNT OF NOISE AND ZERO DRIFT.																		
20																				
21																				

Figure 5-30. 270 VDC Generator Performance Data (3-28-79)

FORM #1300A
AIRESEARCH MFG.

LAB DATA SHEET

Page 2 of 2

EWO 3400-250443-01-0500 DATE 3-29-79 TEST PURPOSE 270 VDC GENERATOR PERFORMANCE

P/N 518988-1-1 BAROM LAB AT SEA LEVEL, ROOM TEMP AMBIENT

S/N R-1 TEMP LAB TEST PERS. S. LEE, J. DEHN, O. KOUYOUMJIAN, S. ROJAS, R. WATERS
J. SEKAART, NADC, E.F. REYNOLDS

TEST POINT	TIME OF DAY	GENERATOR INPUT SPEED RPM.	GENERATOR INPUT TORQUE IN-LB	GENERATOR INPUT HP	GEAR BOX INPUT SPEED RPM	GEAR BOX INPUT TORQUE	GEAR BOX INPUT HP	GENERATOR OUTPUT DC VOLTS	GENERATOR OUTPUT DC AMPS	COOLANT (COOLANOL 25) PRESS OUT PSI	COOLANT PRESS IN PSI	COOLANT FLOW #/HR / GPM	COOLANT TEMP IN °F	COOLANT TEMP OUT °F	GENERATOR BEARINGS REAR TEMP °F	GENERATOR BEARINGS FRONT TEMP °F	CALCULATED GENERATOR η BASED ON HEAT LOSS	CALCULATED GENERATOR HEAT LOSS BTU/MIN	CALCULATED GEAR BOX η % ASSUMED	CALCULATED GEN η BASED ON GEAR BOX EFF.
NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		REMARKS			
22	0935	9000	~~456~~	~~65.4~~	1164	190	63.17	270	153	56	50	613 / 2.6	105	115	145	120	96.4	88.3	91	96.3
23	0941	9000	~~43[illegible]~~	~~62.55~~	1164	188.3	62.61	270	153	56	52	629 / 2.7	114	126	180	129	95.8	102.9		97.2
24	0947	13500	~~262~~	~~56.12~~	1744	131.5	65.51	270	153	102	94	878 / 3.8	130	142	204	140	93.6	160.9		92.9
25	0953	13520	~~26[illegible]~~	~~55.99~~	1748	132.5	66.16	270	153	101	93	882 / 3.8	145	162	250	162	91.0	231.8		92.0
26	1000	176[illegible]	~~205~~	~~57.[illegible]~~	22[illegible]	166.5	69.17	270	153	139	129	1060 / 4.6	160	179	292	180	88.2	313.9		88.0

*

* NOTES

1. TELEMETRY TYPE TORQUE SENSOR DATA IS NOT USABLE DUE TO LARGE AMOUNT OF NOISE & ZERO DRIFT.

2. TEST SETUP SCHEMATIC: TELEMETRY TORQUE SENSOR

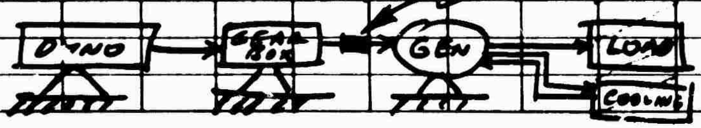
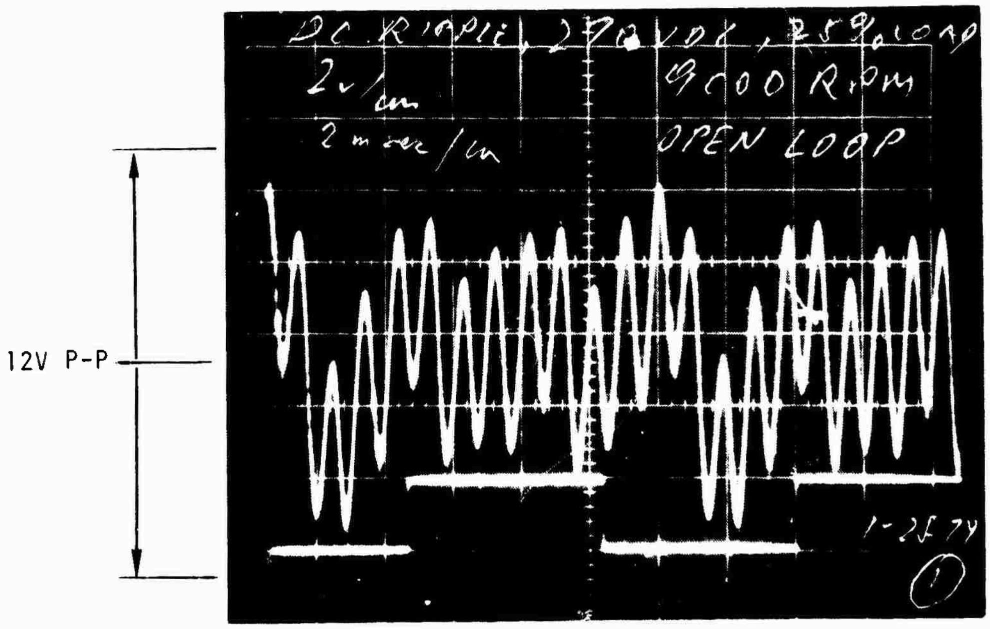
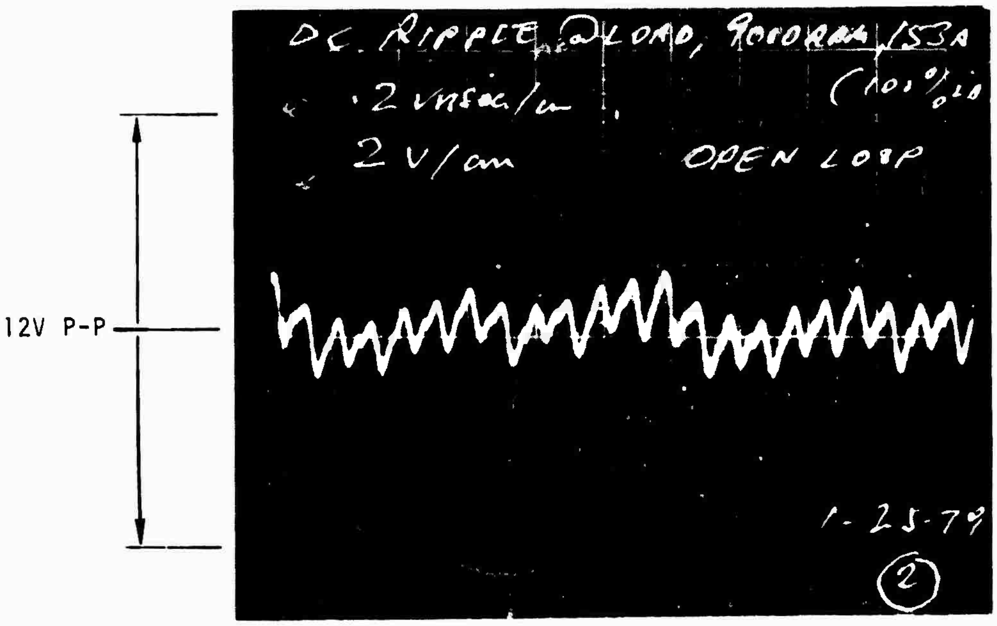


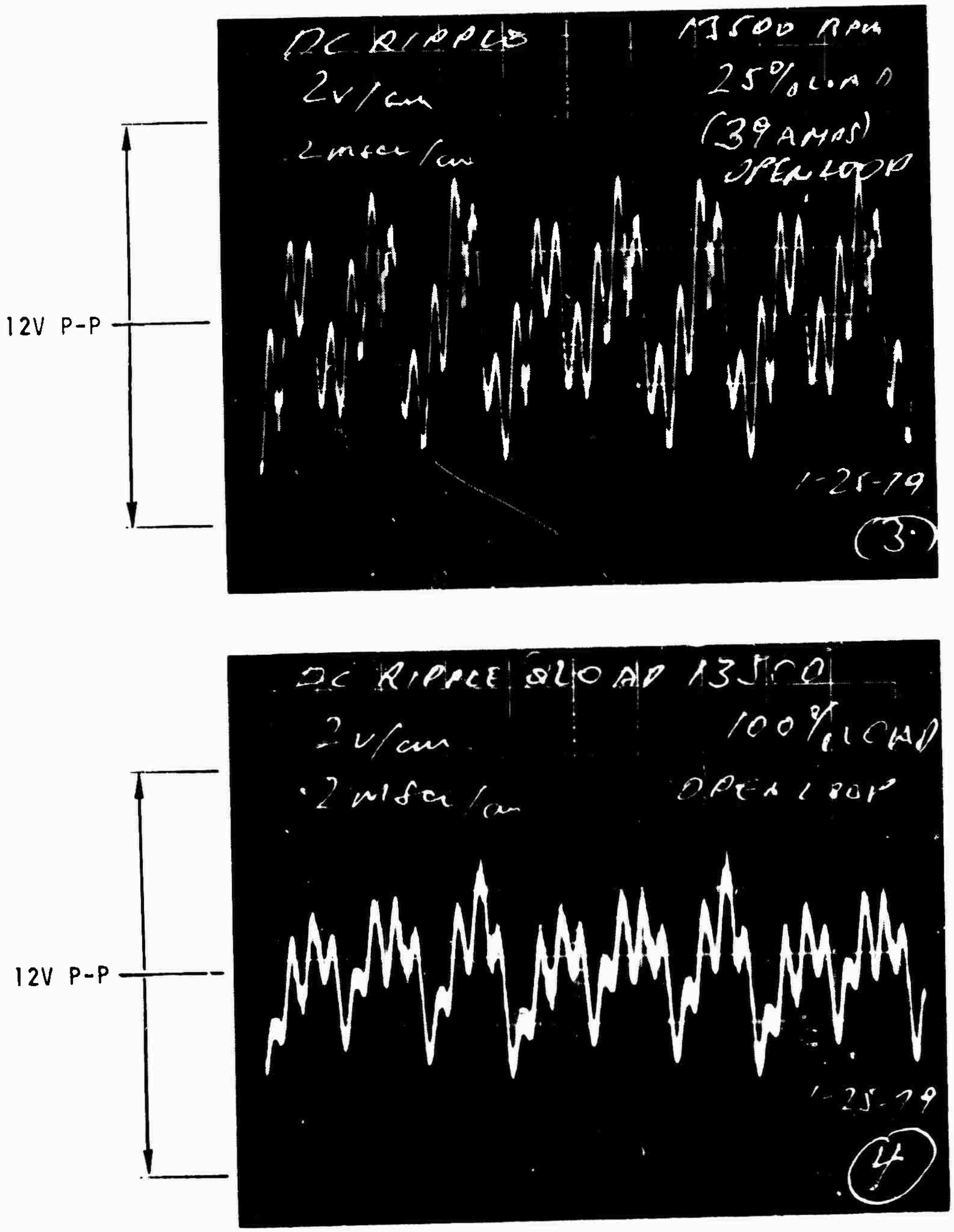
Figure 5-31. 270 VDC Generator Performance Data (3-29-79)





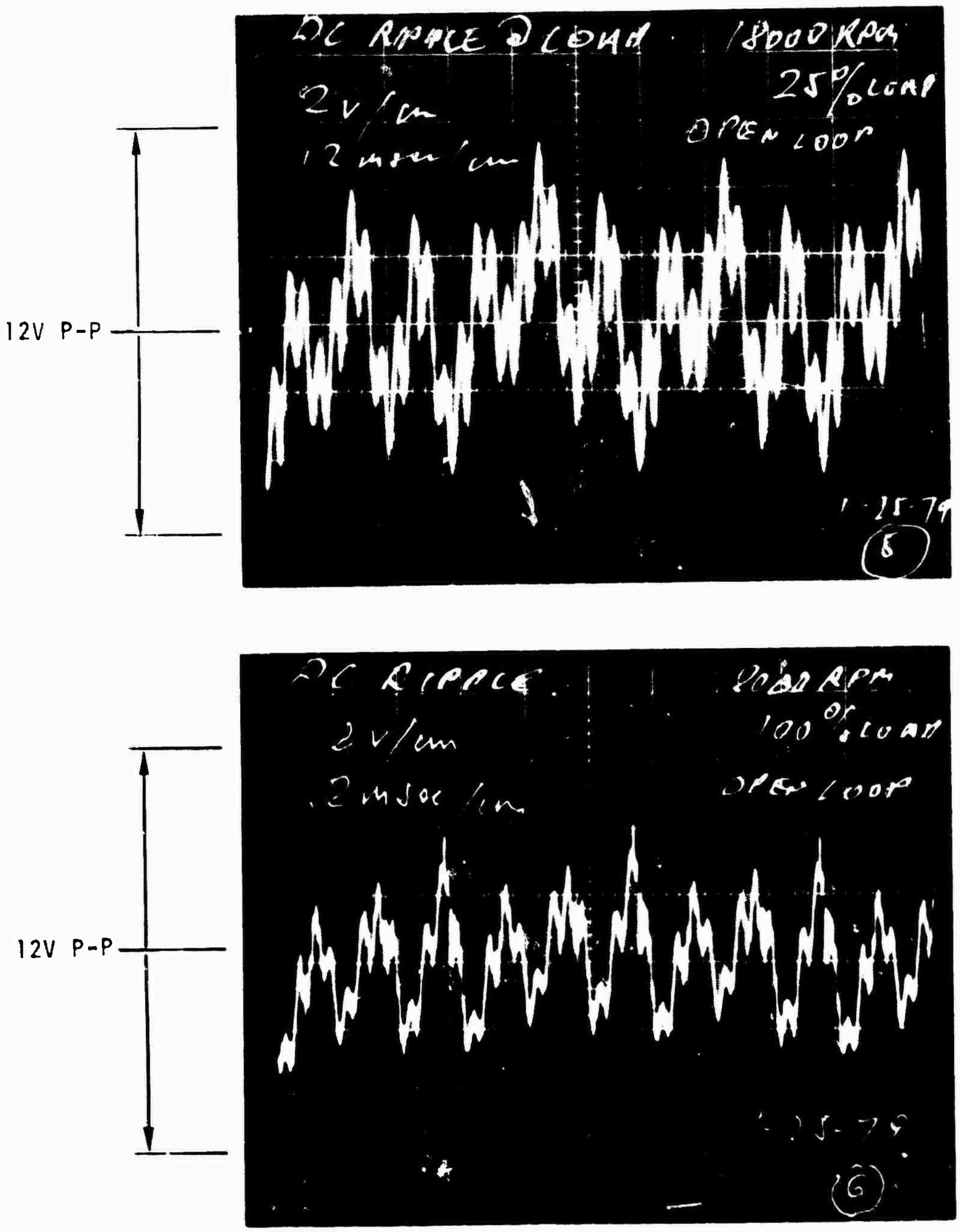
F 29281

Figure 5-32. 270 VDC Generator [illegible], 25 and 100 Percent [illegible]



F 29262

Figure 5-33. 270 VDC Generator Ripple - 13,500 RPM, 25 and 100 Percent Load



F 29251

Figure 5-34. 270 VDC Generator Ripple - 18,000 rpm, 25 and 100 Percent Load

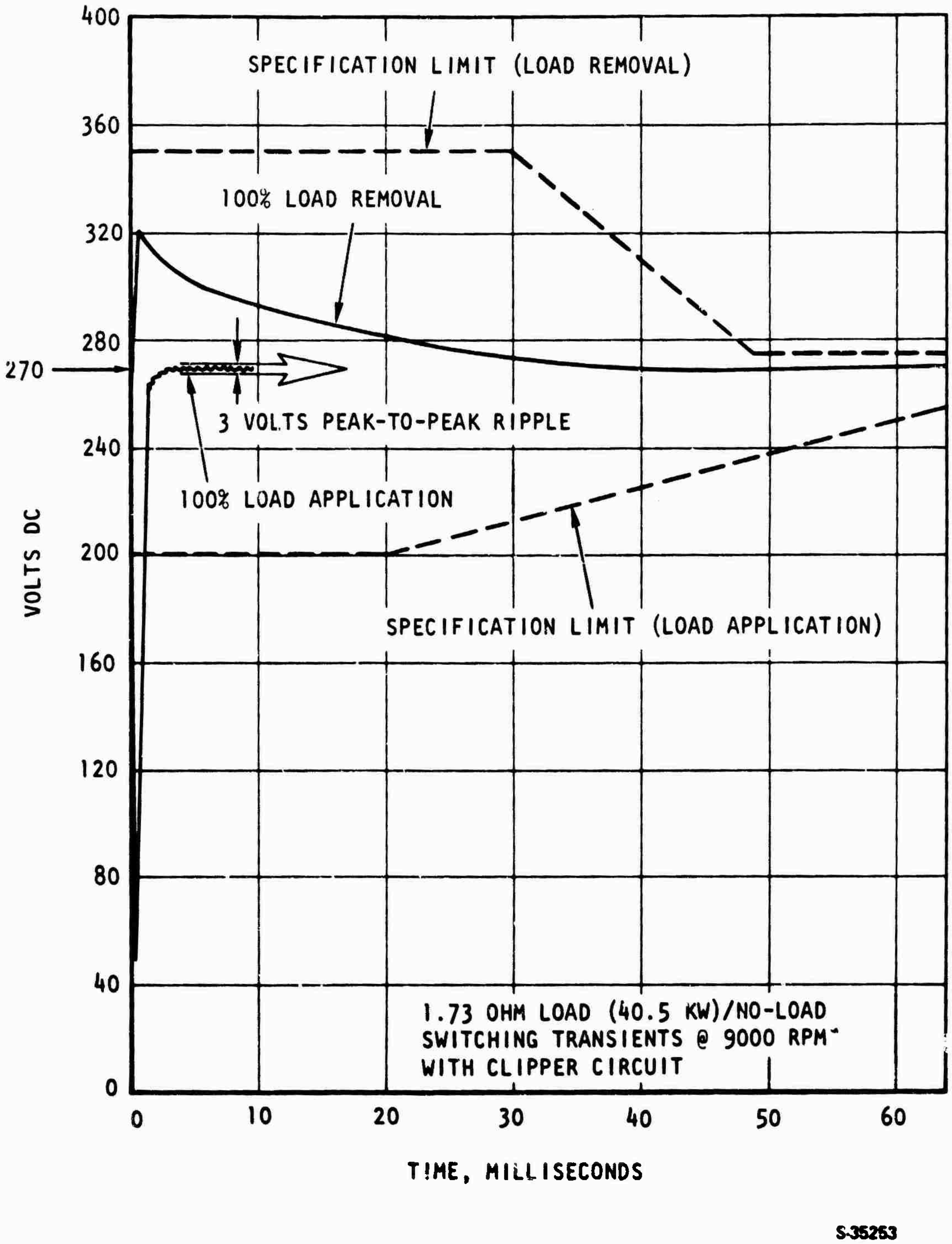


Figure 5-35. Transient Response (100% Load Application and Removal)

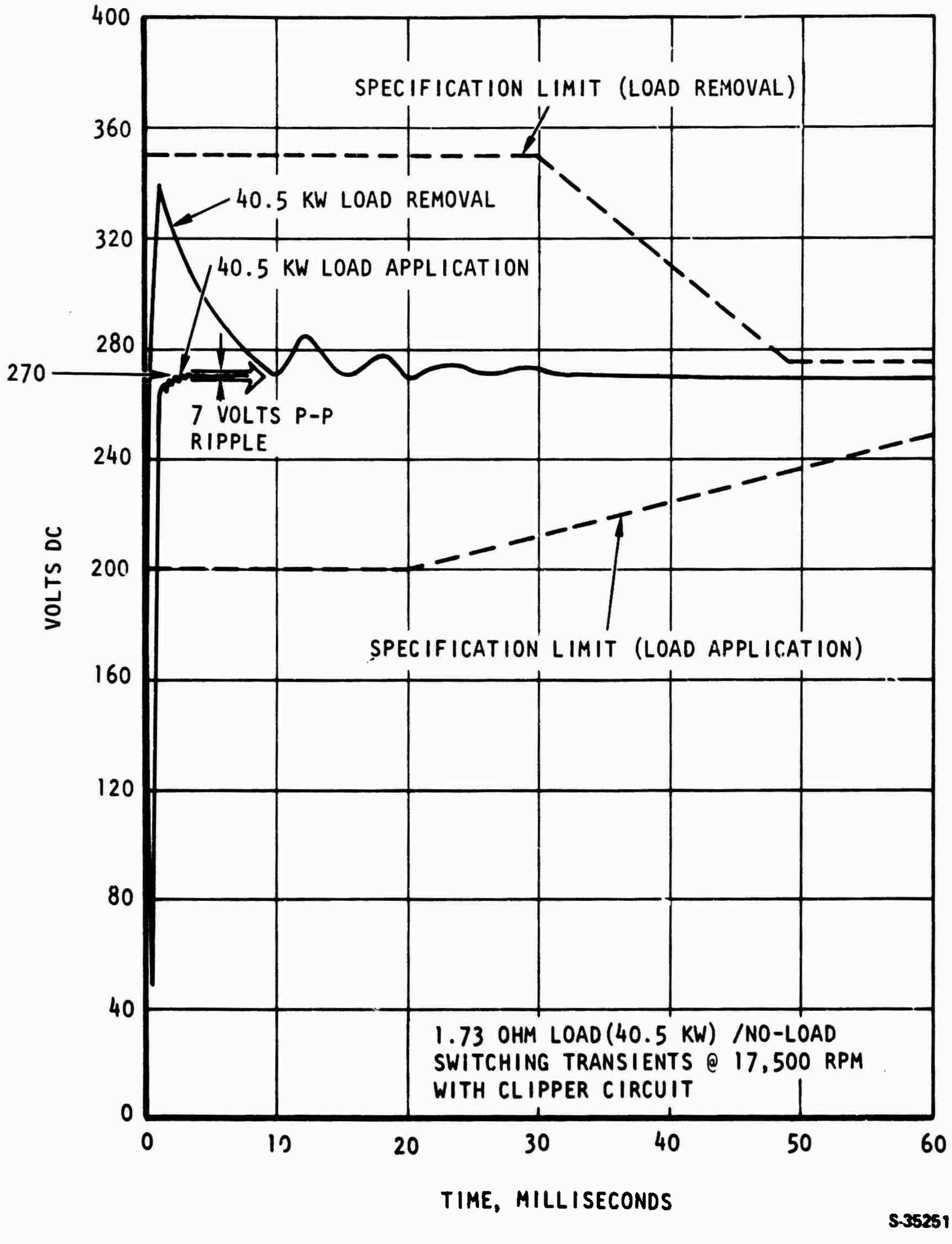


Figure 5-36. Transient Response (40.5 kw Load Application and Removal)

SECTION 6

CONCLUSIONS, RECOMMENDATIONS AND PROPOSALS

During the course of the program it became clear that design and packaging improvements could be made in follow-up units. However, direct changes were not compatible with program schedule and funding at this time. The following paragraphs describe the considerations that should be addressed in the future for follow-up units.

SYSTEM DESIGN APPROACH

Relocation of all electronics is recommended in order to simplify the system and improve reliability. The following areas need additional development to define a flight configuration system:

- Packaging of the voltage regulation and fault protection electronics with the generator as one integral assembly was unsatisfactory because of the vibration and thermal environment imposed on the electronics. Separate packaging of the electronics and mounting in a different location may solve these problems.

- Generator design was too complex with regard to assembly procedures, reliability, and cost.

- Power outputs greater than 45 kw will be required for typical aircraft applications.

- A generator quick-disconnect is required. Since a PM machine generates a voltage whenever it is rotating, it may be necessary to stop the generator to protect it and surrounding equipment in the event of certain fault conditions. Therefore a system is needed to physically disconnect the generator shaft from the driving source. The system would be triggered by the airplane pilot in response to fault signals in the cockpit.

GENERATOR DESIGN AREAS NEEDING FURTHER INVESTIGATION

Stator Cooling Jacket

It has been determined that the use of a bore seal reduces generator weight and size, but due to added complexity and cost, it is not the best production approach. The use of a stator cooling jacket integral with the main housing will increase weight and size; however, it is simpler and less costly.

Bearing System Design

The use of an enclosed, separate oil wick-lubricated bearing design has been shown to be an effective solution for high DN, high temperature applications. A possible simpler alternate may be the oil mist-lubricated bearing design in conjunction with the cooling scheme.

Auxiliary Winding Adjustment

Test data have shown that the auxiliary stator approach works well and should be utilized in production hardware. Mechanization of the auxiliary and main winding alignment needs some improvement to simplify assembly procedures.

Cooling Pump

Feasibility of a pitot pump for unpressurized case, all-attitude start and operating condition had been demonstrated. Investigation of other type pumps with a pressurized pump may result in an improved cooling and lubricating system.

High-Speed Quick-Disconnect

After initial problems with an integral design quick-disconnect, a reassessment of the task was made, and the following design requirements were established after consulting with Naval Air Test Center Engineering:

- Completely decouple from gearbox in approximately 0.010 sec for 7,000 to 18,000 rpm speed range, no-load to full load.
- No false trips allowed due to vibration, shock, or high g loading.
- After decoupling, latch in disconnect position without possibility of automatic reconnection while input pad is operating.
- External indication of disconnect status is required without generator removal from mounting pad.
- Disconnect has to be manually resettable without removing from pad and positive indication of fully engaged position is required.
- Generator to be fully operational after cycling disconnect mechanism 10 times (cycle = disengage at full speed of 18,000 rpm, shutdown, reset, bring back to full speed).
- Ambient: -65° to 250°F, max mechanism temp: 400°F

AiResearch is investigating a sandwich type quick-disconnect adaptable to the 270 VDC generator.

COMPONENT DESIGN APPROACH

Repackaging of the ripple inductor and the interphase transformer is recommended to reduce weight.

The cooling pump rotating cup impeller blade design will be modified to single-piece construction. The present unit utilizes a two-piece bonded assembly, and it also should be replaced with a single-piece bladed impeller as soon as practical.

THYRISTOR OPTIMIZATION

The currently designed SCR is a standard configuration with the threaded stud and flats machined from it. The resulting slug is soldered to an aluminum pin fin heat exchanger and subsequently a cover is soldered to the heat exchanger. These solder operations threaten the integrity of the SCR chip-to-heatsink bond.

For future production it is recommended that the header be completed with its heat sink prior to bonding of the SCR chip. This approach offers fewer risks and better cooling, since at least one thermal barrier is eliminated.

APPENDIX A

SPECIAL TEST EQUIPMENT FOR 270 VDC GENERATOR SYSTEM

Special test equipment was required to build and test both the rotating machine and the control box, as follows:

- Generator Control Unit (GCU) Test Panel, PN SK43199
- Generator Cooling Loop
- Vi-Star Model 6513-3 Step-up Gearbox, 7.7462:1 ratio
- Internal Transmitter Coupling for Acurex Telemetry Torque Sensor
- Generator Mounting Angle Plate, PN LSK15173
- System Load Bank, PN LSK15976 (load switching in 25-percent steps)
- Generator Rotor Overspeed Fixture (also used for handling of highly magnetized rotor during assembly)

The following paragraphs describe the GCU Test Panel and the Generator Cooling Loop.

GENERATOR CONTROL UNIT (GCU) TEST PANEL, PN SK43199

The 270 vdc GCU test panel was designed primarily to assist in the development of hardware and software for the generator control unit prior to its interconnection with the generator. The test panel was also useful during runs with the generator.

To understand the operation of the test panel it is necessary to know that the GCU has three connectors--J1, J2, J3. The first two connectors, J1 and J2, are used for interfacing with the generator; J3 is used for interfacing with the cockpit, the 270 vdc bus, and the different current sensors. The features of the test panel associated with J1 and J2 will not be operational when the GCU is connected to the generator. Figure A-1 shows the test panel schematic.

Some of the LED (light-emitting diode) indicators and jacks provided on the test panel monitor internal signals within the GCU. A distinction will be drawn between these and other signals as the various features of the test panel are discussed.

The three-position OFF-TEST-ON switch and the indicator light marked GSI (generator status indicator) are as described in Section 3.6.2.1 of specification NADC-VT-TS-7502, henceforth referred to as the spec. The GSI light simulates the generator warning light referred to in the spec.

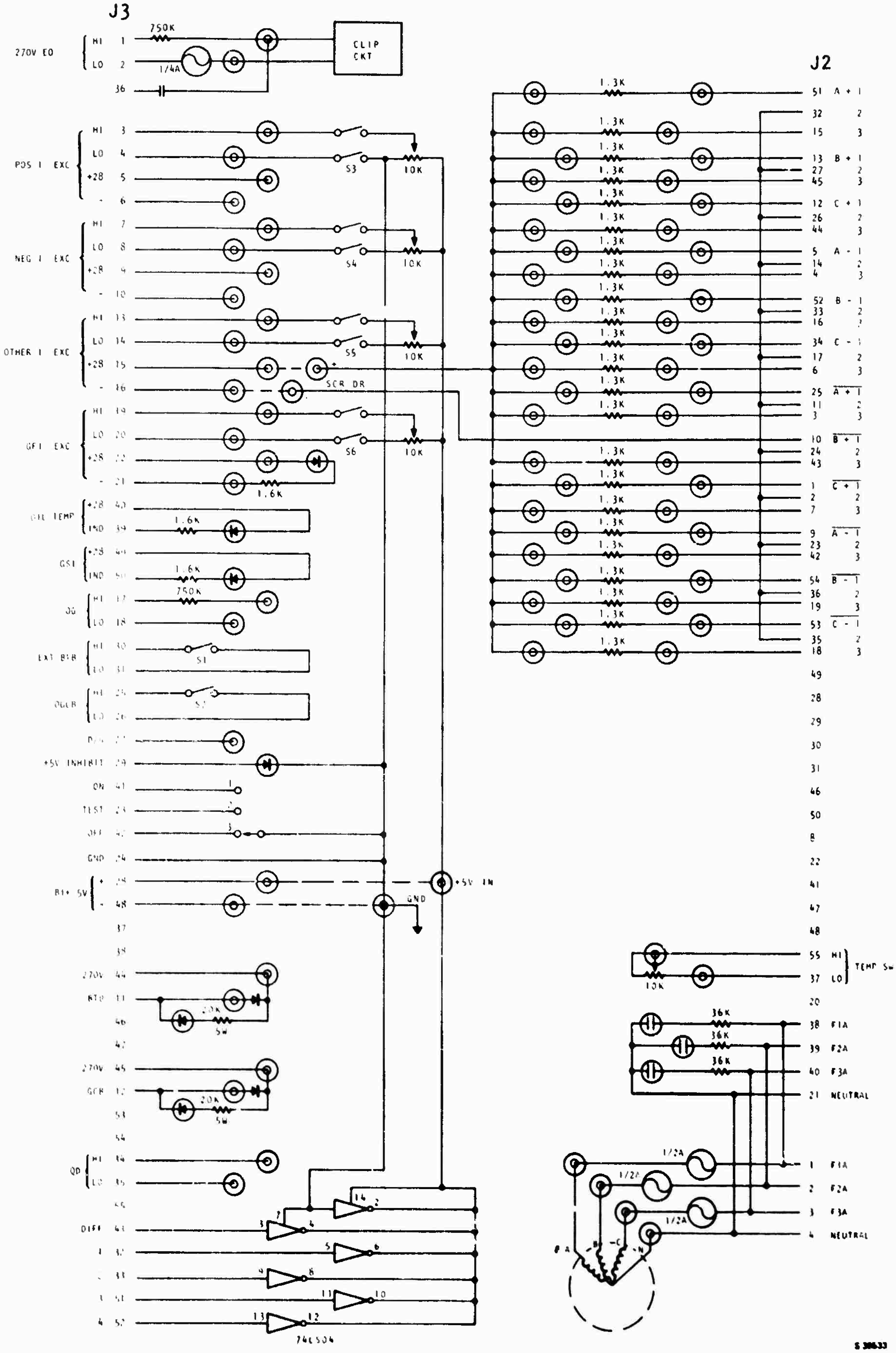


Figure A-1. GCU Test Panel Schematic

Switch S1, marked EXT BTB, controls the bus tie breaker. When this switch is in the "1" position the bus tie breaker is turned on; otherwise the bus tie breaker is turned off. The indicator light marked BTB indicates the status of the bus tie breaker; it is on when the bus tie breaker is on. The two jacks marked BTB and 270V BTB should be connected to the bus tie breaker if one is used in the system. There is a GCU generated 270V supply available at the 270V BTB jack. The jack marked BTB is the open collector output of a power transistor inside the GCU.

The jacks marked GCB and 270V GCB are similar to the jacks discussed in the preceding paragraph except that they are used to control the generator circuit breaker which is in series with the load. The LED indicator marked GCB indicates the state of the generator circuit breaker. The light is on when the GCB is turned on.

Switch S7, marked OGCB, simulates the auxiliary outputs of a circuit breaker of a second generator connected in parallel with the first generator. When the switch is in the "1" position, this is equivalent to having the second generator on the bus.

The LED indicator marked OIL TEMP provides a signal as described in Section 3.5.5 of the spec.

There are four current sensors which interface with the GCU. These are POSI, NEGI, EGFI (ground current), and OTHERI (current supplied by the second generator). Each sensor interfaces to the GCU through four terminals. Two of these are +28V and +28V return which are generated by the GCU. The other two provide a voltage output from the sensor to the GCU. Thus there are four jacks on the test panel for each current sensor. The excitation to the ground current sensor differs slightly from the others in that the 28V return is the open collector of a transistor rather than GCU ground.

An indicator light, GFI, is on when the 28V excitation return path is closed (i.e., current can flow). The four pots marked POSI, NEGI, OTHERI and EGFI can be used to simulate sensor outputs. The pot outputs are applied as inputs to the GCU only when their respective switches (S3, S4, S5, S6) are flipped to the right. A +5V supply provided on the test panel (BI + 5V HI and BI + 5V LO) can be used to excite these pots and provide power to the LED indicators on the test panel. To do this, BI + 5V HI should be tied to +5V IN and BI + 5V LO tied to GND.

The light marked DIFF is turned on when the bus voltage is above or below 270 volts by more than 5 volts.

The lights marked F1, F2, F3, F4 indicate the reason for shutdown if such an action is taken by the GCU. The following table summarizes the different faults.

F4	F3	F2	F1	Fault
0	0	0	0	No fault
0	0	0	1	POSI/NEGI > 35%
0	0	1	0	POSI > 150%, 7 seconds
0	0	1	1	Ripple > 24V p-p, 200 msec
0	1	0	0	Ground Current > 5 ma, 30 msec
0	1	1	0	Underspeed
1	0	0	0	EO < 240V, 6 seconds
0	1	1	1	EO > 290V, 200 msec
1	1	1	1	POSI > 170%, 40 msec

Concerning the underspeed indication, the reference speed is 9000 rpm or 7000 rpm, depending on the status of the generator. If the generator is not on the bus, then underspeed will be indicated for as long as the speed is less than 9000 rpm and the generator will not be turned on. Once the speed reaches 9000 rpm, the underspeed indication is blanked. When the generator has been running and the speed drops below 7000 rpm, the generator is shut down and lights F2 and F3 are turned on.

The 270 VDC bus terminals can be plugged into the two jacks marked 270V EO HI and 270V EO LO. There is a 1/4-amp fuse in series with the 270V EO LO terminal. A clipper circuit is mounted on the test panel in parallel with the 270 VDC bus. This clipper circuit clamps any spikes to 350 volts. Figure A-2 is a schematic of the clipper circuit.

The jack marked D/A is used for monitoring an internal reference signal within the GCU. The LED indicator marked +5V INHIBIT indicates the state of an internal electronic switch.

HOOK-UP INSTRUCTIONS

Figure A-3 depicts the test setup. A wire should be run from the high end of the 270 VDC bus to the jack on the test panel marked 270V EO HI. Another wire should be run from the low end of the 270 VDC bus to the jack on the test panel marked 270V EO LO. The OFF-TEST-ON switch can be switched to either TEST or ON position. In the TEST position, the generator circuit breaker will not be allowed to close (i.e., the generator will not be connected to the load bank).

BI + 5V HI should be jumpered to +5V IN and BI +5V LO should be jumpered to the jack marked GND.

The cable marked J3 should run from the J3 connector on the GCU to the J3 connector on the test panel. The J2 connector on the panel should not be used.

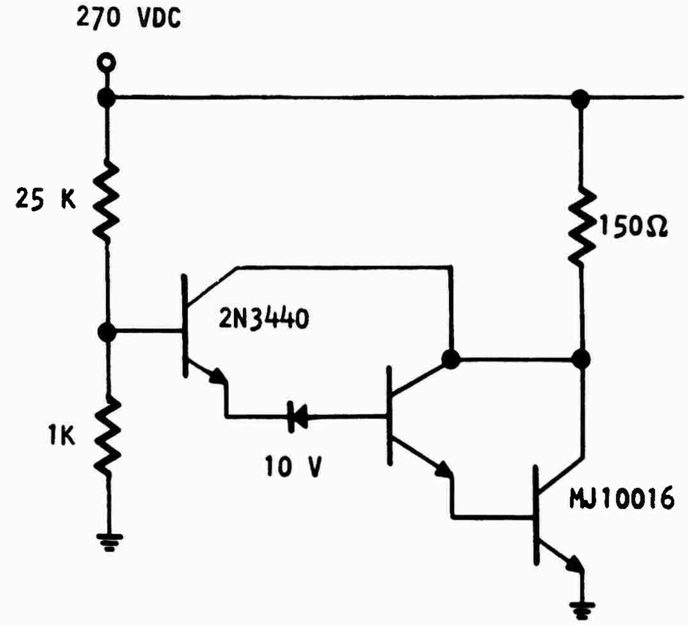


Figure A-2. Clipper Circuit Schematic

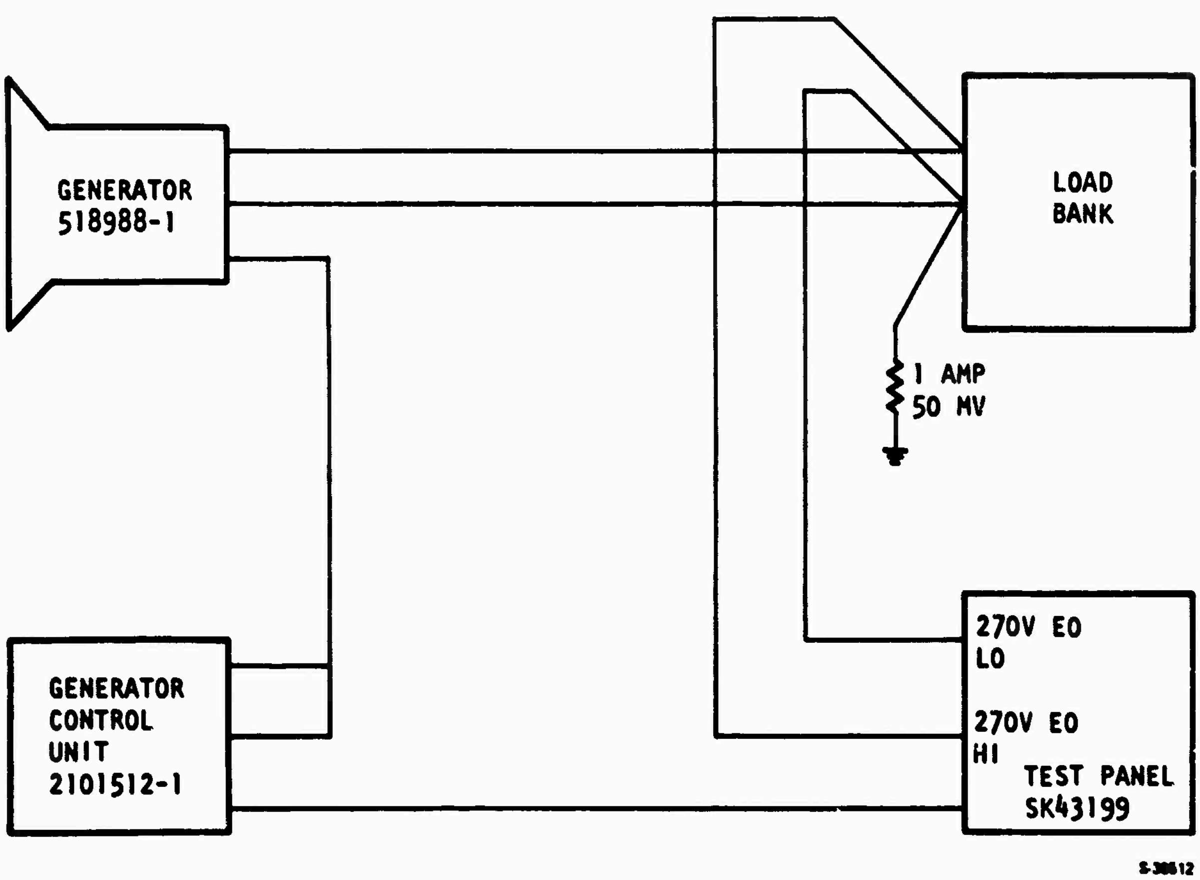


Figure A-3. 270 VDC Generator Electrical Hookup

The interconnections between the current sensors and the test panel are described in a preceding paragraph. If current sensors are used, the simulated pot inputs (POSI, NEGI, OTHERI, GFI) should be disabled by flipping S3, S4, S5, S6 switches to the left position. The jacks marked GCB and 270V GCB (this is an internally generated 270 volts) should be used to interconnect to the circuit breaker. Any time there is a fault and the generator is shut down, the unit must be reset by flipping the OFF-TEST-ON switch to the OFF position and back to the TEST or ON position.

When the test panel is not connected the user should be aware of the fact that some of the signals available on J3 are used for internal monitoring of the GCU only.

270 VDC GENERATOR COOLING LOOP

The cooling loop in its final configuration is shown in Figure A-6. Figures A-4 and A-5 and the following paragraphs describe the servicing procedure used to charge the system.

(a) Pull vacuum on system as shown in Figure A-4.

(b) Turn on external circulating pump and cycle fluid through cooling system on de-airator.

(c) Turn off servicing pump and connect generator to servicing system as shown in Figure A-5.

(d) Adjust servicing pressure to 10 ± 5 psig, monitor sight glass on generator reservoir, and fill to top of glass.

(e) Disconnect service lines and connect generator to cooling system as shown in Figure A-6.

(f) Release pressure build-up from servicing on top of generator reservoir.

(g) Run generator at approximately 2000 rpm and monitor reservoir fluid level, system flow, and pressure. Air bubbles should disappear in a very short time, and flow pressure indication should be steady. Output flow should be 0.2 to 0.3 gpm, output pressure approximately 3 psig.

(h) Increase speed to 9000 rpm, while continuously monitoring flow and pressure. There should be smooth acceleration with no sudden flow or pressure changes. At 9000 rpm, flow reading should be 2.3 to 2.7 gpm with output pressure at 45 to 60 psig, depending on coolant temperature.

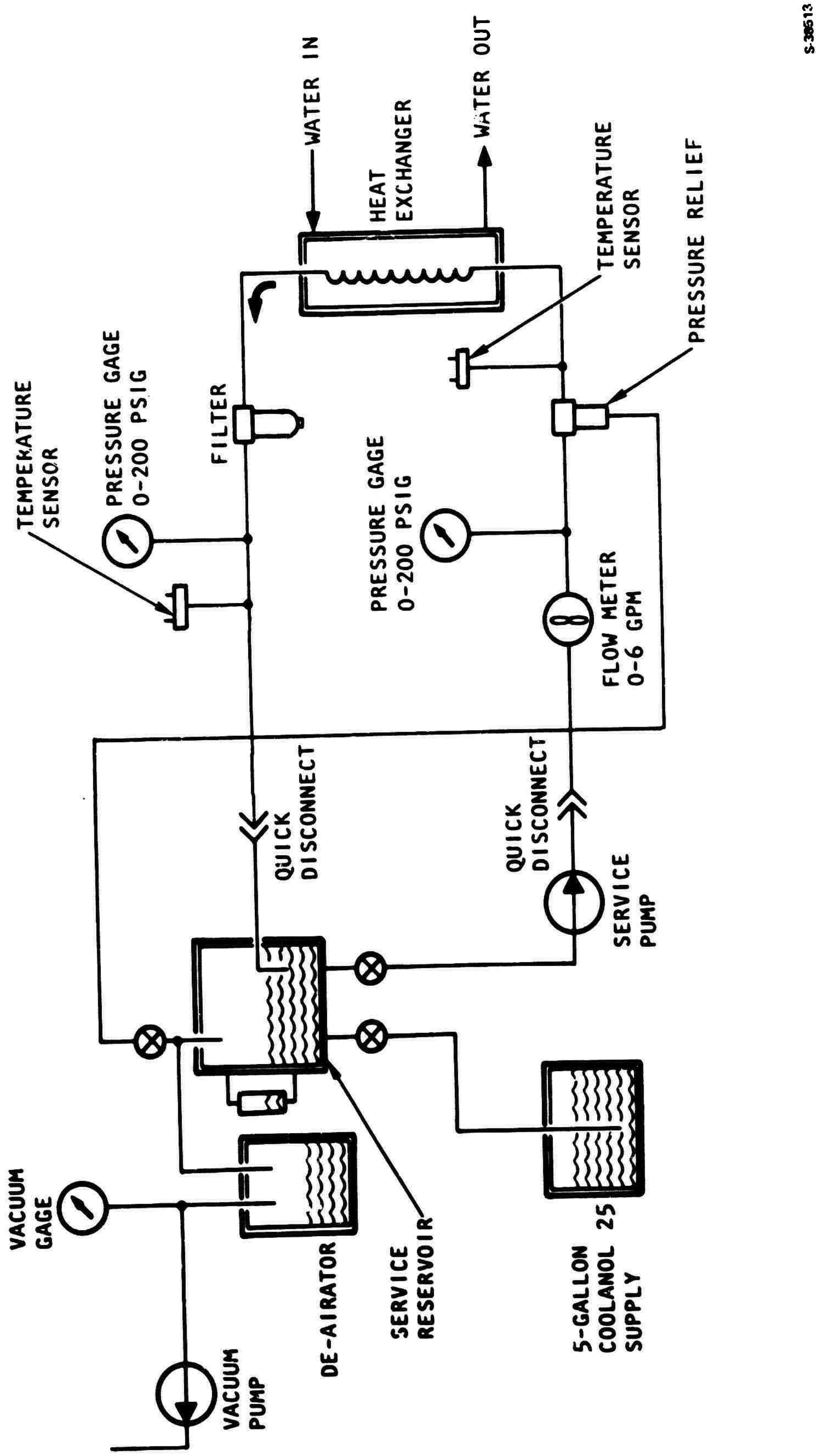


Figure A-4. Cooling Loop Servicing (Before Connecting Generator)

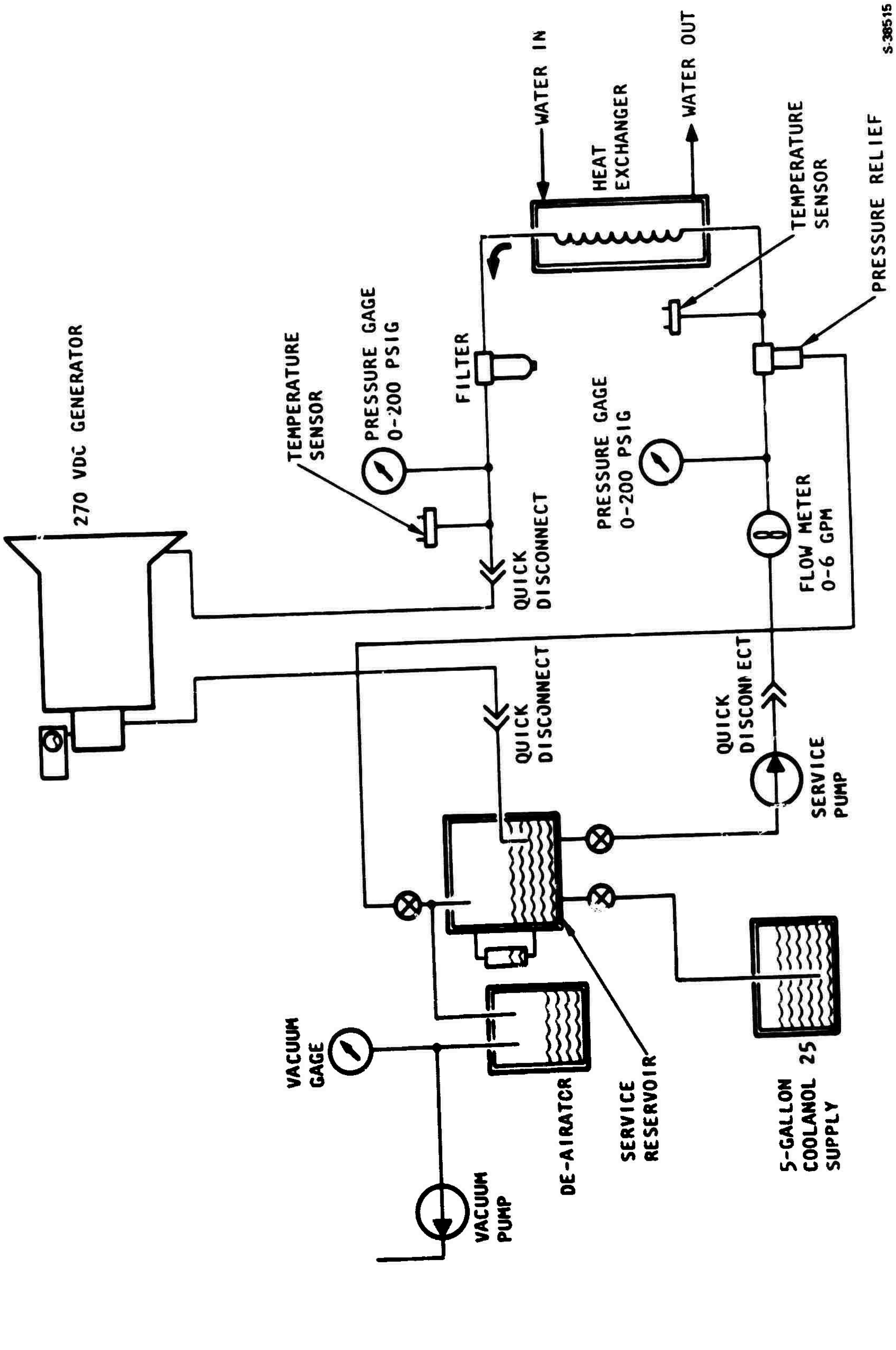


Figure A-5. Cooling Loop Servicing (Generator Connected)

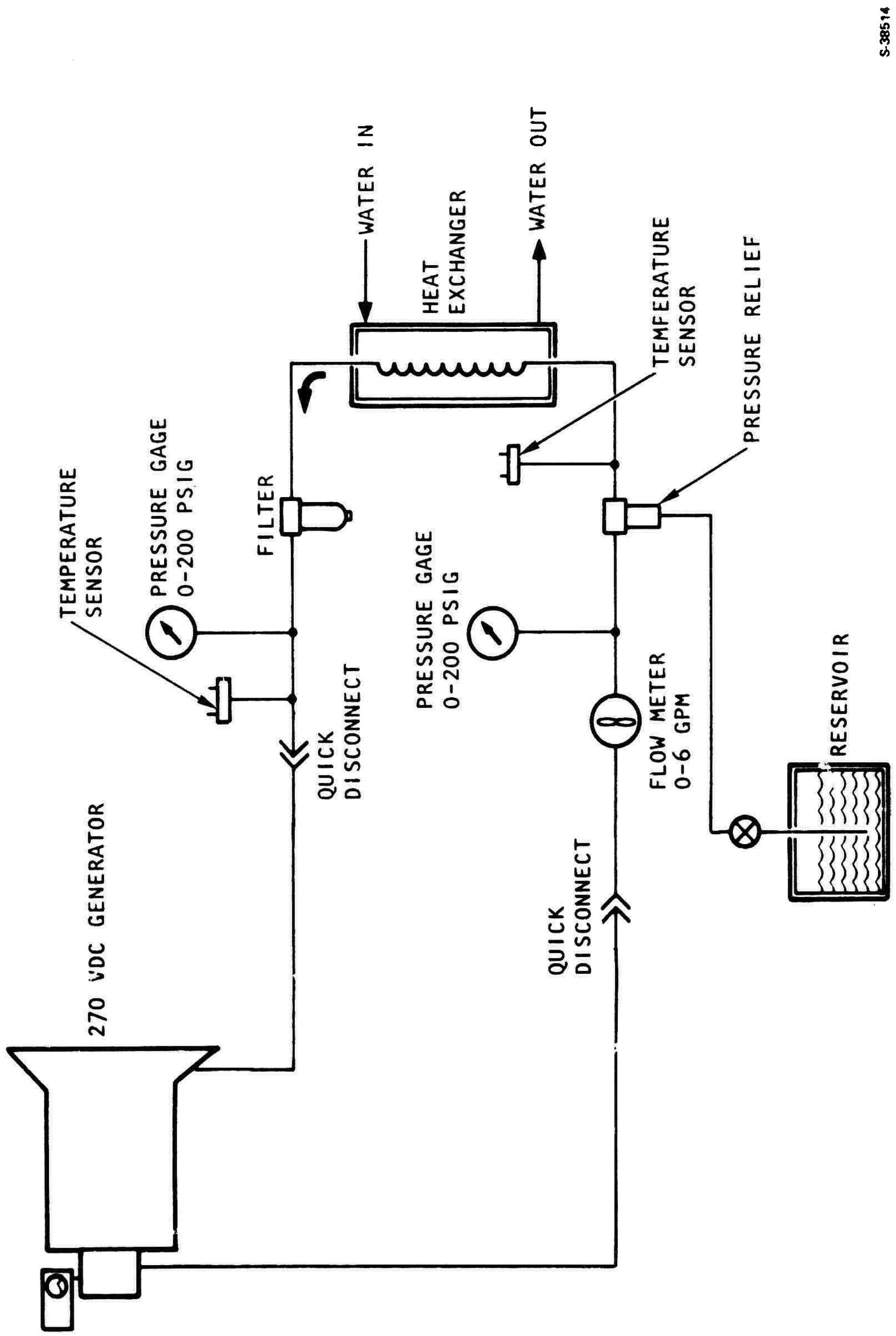


Figure A-6. Final Configuration of Generator Cooling Loop

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